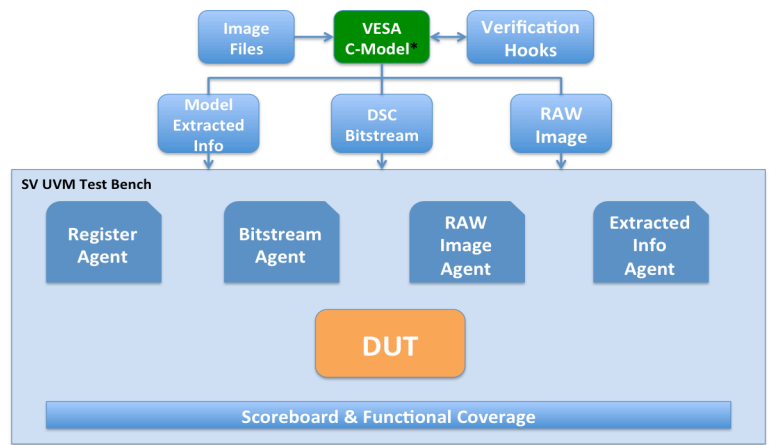


VESA DSC 1.1 Video Encoder and Decoder Verification IP



* Available for download on VESA members website

Why use a proven verification IP?

- Lowers project risk
- Verifies designs quickly and thoroughly
- Speeds up debugging
- Reduces development costs
- Supports industry standards for greater interoperability

Hardent provides IP solutions as well as cutting-edge ASIC and FPGA design services for electronics manufacturers using display technology. As a member of VESA and a key contributor of the DSC Task Group, Hardent has used its expertise and skills to develop the very latest standards in display technology. Hardent's high-quality IPs enable clients to accelerate their development schedules and meet demanding time-to-market deadlines.

Key Features

- Supports all mandatory and optional VESA DSC v1.1 features
- Based on the latest VESA C-model version 1.31
- SystemVerilog UVM 1.1d compliant verification environment
- Constrained random test bench
- Functional test library
- Functional coverage
- Test plan and coverage plan
 - Compliance tests
 - Based on typical usage models
 - Explore key register/parameter combinations
 - Randomized register/parameters with functional coverage to test robustness and corner cases
- Protocol checking with assertions
- Debugging tools

Deliverables

- Complete test bench and UVM verification environment
 - Agents (Sequencers, Drivers, Monitors)
 - Virtual sequencer and sequence library
 - Scoreboard and functional coverage
- Comprehensive image library and test suite
 - Real life, graphics, patterns and random
 - Standard resolutions and aspect ratios
 - Odd-sized, partial groups, multiple slices per line
- Random image generator (size/content)
- Detailed user guide

Product options

- Technical support and maintenance updates
- Customization, integration, compliance tests and debugging services available on request

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