General Description

The Digital Blocks DB6845 CRT Controller core is a full function equivalent to the Motorola MC6845 device. The DB6845 interfaces a microprocessor to a raster-scan CRT display. The microprocessor access 19 registers (1 Address and 18 Data Registers) within the DB6845 in order to provide video timing, refresh memory addresses, cursor, and light pen strobe signals. CRT video timing signals include Vertical Sync (VS), Horizontal Sync (HS), and Display Enable (DE) output signals. Refresh memory addressing includes Memory Address (MA[13:0]) and Row Address (RA[4:0]) output buses.

Features

- Synchronous, synthesizable VHDL Core, functionally equivalent to Motorola MC6845.
- Capable of driving alphanumeric, semi-graphic, or bit-mapped graphics displays. Wide range of programmable screen formats.
- Programmable registers controlling output signals Vertical Sync (VS), Horizontal Sync (HS), and Display Enable (DE) signals. Programmable horizontal line rate and sync pulse width. Programmable vertical frame rate.
- Programmable registers controlling Memory Address (MA[13:0]) start address. Programmable Start Address Register for Hardware Scrolling.
- Programmable registers controlling Row Address (RA[4:0]) size, yielding a character row.
- Programmable register controlling Normal Sync (Non-Interlace), Interlace Sync, or Interlace Sync & Video Mode.
- Programmable registers for control and format of Cursor.
- Light Pen Register.
- Microprocessor 8-bit Data Bus and Control Interface.

Block Diagram

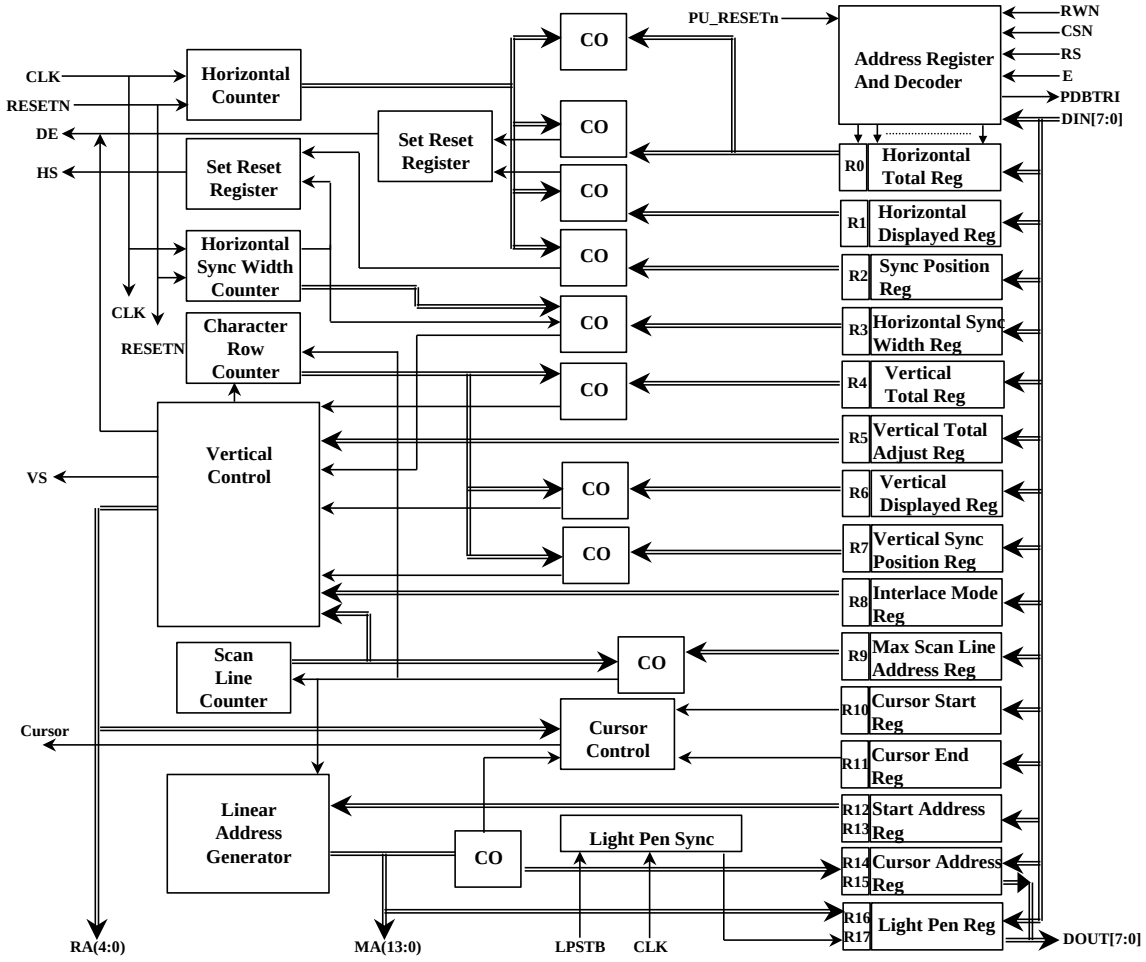

Figure 1: DB6845 CRT Controller Block Diagram

Register Assignment

CSn	RS	Address Register [4:0]	Reg. No.	Register Name	Program Unit	R/W	Data Bit D[7:0]							
1	-	-	-	-	-	-								
0	0	-	AR	Address Register	-	W								
0	1	00000	R0	Horizontal Register	Character	W								
0	1	00001	R1	Horizontal Displayed	Character	W								
0	1	00010	R2	H. Sync Position	Character	W								
0	1	00011	R3	Sync Width	-	W								
0	1	00100	R4	Vertical Width	Character Row	W								
0	1	00101	R5	V. Total Adjust	Scan Line	W								
0	1	00110	R6	Vertical Displayed	Character Row	W								
0	1	00111	R7	V. Sync Position	Character Row	W								
0	1	01000	R8	Interlace Mode & Skew	-	W							I1	I0
0	1	01001	R9	Max Scan Line Address	Scan Line	W								
0	1	01010	R10	Cursor Start	Scan Line	W		B	P					
0	1	01011	R11	Cursor End	Scan Line	W								
0	1	01100	R12	Start Address (H)	Memory Address	W	0	0						
0	1	01101	R13	Start Address (L)	Memory Address	W								
0	1	01110	R14	Cursor (H)	Memory Address	R/W	0	0						
0	1	01111	R15	Cursor (L)	Memory Address	R/W								
0	1	10000	R16	Light Pen (H)	Memory Address	R	0	0						
0	1	10001	R17	Light Pen (L)	Memory Address	R								

Table 1: DB6845 CRT Controller Internal Register Assignments

Functional Description

The DB6845 CRT Controller core is partitioned into modules as shown in Figure 1 and described below.

Horizontal Timing

In Figure 1, the Horizontal Timing section consists of the Horizontal Counter, Horizontal Sync Width Counter, Registers R0 through R3, and associated synchronous Set/Reset Flip-Flops and Coincidence Circuits.

The Horizontal Counter counts from zero until coincidence with Register R0 synchronously resets the counter. This represents the horizontal line rate and enabling of the Display Enable (DE) for a new line takes place.

Coincidence of the Horizontal Counter with Register R1 marks the end of the active display portion of a horizontal line with Display Enable (DE) going inactive.

Coincidence of the Horizontal Counter with Register R2 marks the beginning of horizontal retrace with Horizontal Sync (HS) going active high.

Coincidence of the Horizontal Sync Width Counter with Register R3 marks the end of horizontal retrace with Horizontal Sync (HS) going inactive low.

Vertical Timing

In Figure 1, the Vertical Timing section consists of the Scan Line Counter, Character Row Counter, Registers R4 through R9, the Vertical Control logic block, and associated Coincidence Circuits.

The Scan Line Counter counts from zero until coincidence with Register R9 synchronously resets the Scan Line Counter and synchronously increments the Character Row Counter. The Scan Line Counter counts the Scan Lines composing a character row, and the Character Row Counter counts the character rows comprising a vertical frame.

The Character Row Counter coincidence with R4 and the residual Scan Line count represented by R5 marks the end of a vertical frame.

The Character Row Counter coincidence with Register R6 marks the end of the active display portion of the vertical frame measured in character rows.

The Character Row Counter coincidence with Register R7 marks the beginning of vertical retrace with Vertical Sync (VS) going active high. VS remains high for a fixed period of 16 scan lines.

Register R8, Interlace Mode Register, affects the Vertical Timing according to its programming. Normal Sync (Non-Interlace) mode displays the same field each frame.

Interlace Sync Mode splits a frame into even and odd fields. Vertical Sync (VS) active high is delayed one-half scan line at the end of even fields. For Interlace Sync & Video Mode, in addition to the VS delay on even fields, the Row Address counter sequences on even fields through 0, 2, 4, … counter values while on odd fields, through 1, 3, 5, … counter values.

Cursor

In Figure 1, the Cursor section consist of the Cursor Control, Cursor Start Register R10, Cursor End Register R11, Cursor Address Registers R14 and R15, and associated Interlace Mode Register settings and Refresh Memory Address and Row Address buses as well as associated Coincidence Circuits.

As a first condition for activating the cursor, Cursor Address Registers R14 and R15 signify the character in linear address space the cursor can be active. Then, Cursor Start Register R10 and Cursor End Register R11 select the scan lines within the designated character space the cursor will be active.

In addition, Cursor Start Register R10 contains a 2-bit field indicating whether the cursor is active or not, and, if so, whether it should blink or not, and, if blink, at 1/16 th or 1/32 nd the field rate.

Start Address

Start Address Register R12 and R13 indicate the first address the Linear Address Generator puts on the Refresh Memory Address bus at the start of a vertical frame. Whenever the microprocessor writes to R12 and R13, the Linear Address Generator is updated at the start of the next vertical frame.

Light Pen Register

On the rising edge of the LPSTB input, after synchronization by two CLK cycles, the value of the Refresh Memory Address bus is captured by the Light Pen Registers R16 and R17. These registers are readable by-way-of the microprocessor interface.

Linear Address Generator

The Linear Address Generator generates the Refresh Memory Address. The Linear Address Generator initializes to the value of the Start Address Registers R12 and R13 at the start of each vertical frame. The Linear Address Generator remains active during horizontal and vertical retrace, for refresh of dynamic RAMs

Verification Methods

The DB6845 CRT Controller cores function & timing were verified by means of a prototype board containing the Motorola MC6845 and the DB6845 in an FPGA. Both CRT Controller’s registers were loaded and the results captured by a logic analyzer.

Inputs and outputs were then compared on a cycle-by-cycle basis using compare scripts. The DB6845 has been verified in silicon via customer designs.

Pin Description

Name	Type	Polarity	Description
Microprocessor Interface			
DIN[7..0]	IN	-	Data Bus Input
DOUT[7..0]	OUT	-	Data Bus Output
PDBTRI	OUT	(See Description Below)	Processor Data Bus Tri-state Control H= Processor Reads L= Processor Writes
RS	IN	Low	Address Register Select
		High	Data Register Select
RWn	IN	Low	Write to Internal Register
		High	Read Internal Register
CSn	IN	Low	Chip Select
E	IN	High	Enable Data Bus Output During Microprocessor Reads
		Falling Edge	Register Data During Microprocessor Writes
Light Pen Strobe Interface			
LPSTB	IN	Rising Edge	Light Pen Strobe
Reset and Clock Interface			
RESETn	IN	Low	Reset/Test Mode
CLK	IN	Falling Edge	Synchronous Clock (Except for Micro-processor Interface)
PU_RESETn	IN	Low	Asynchronous Power-up Reset
CRT Control Interface			
DE	OUT	High	Display Enable
HS	OUT	High	Horizontal Sync
VS	OUT	High	Vertical Sync
Refresh Memory/Character Generator Addressing Interface			
MA[13..0]	OUT	-	Refresh Memory Address
RA[4..0]	OUT	-	Row Address
Cursor Interface			
CURSOR	OUT	High	Cursor

Table 2: DB6845 CRT Controller I/O Pin Description

Notes to Table 1:

1. If DB6845 bus wrapper employed, buses DIN[7:0] and DOUT[7:0] and signal PDBTRI replace the MC6845 bi-directional data bus D[7:0].

Related Information

Motorola MC6845 CRT Controller Datasheet. Please contact Digital Blocks for a copy.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, and support information.

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