General Description

The Digital Blocks DB-FPD-LVDS-TX LVDS Display Interface IP Core interfaces parallel 18-bit/24-bit RGB Pixel Data with display timing VSYNC, HSYNC, Data Enable, and Pixel Clock to a FPD LVDS compliant display panel via 3 or 4 LVDS Differential Data Pairs and 1 LVDS Differential Clock Pair.

Figure 1 depicts the top level block diagram of the DB-FPD-LVDS-TX LVDS Display Interface IP Core embedded within an integrated circuit device, interfacing an internal Display Controller to an external LCD Display Panel.

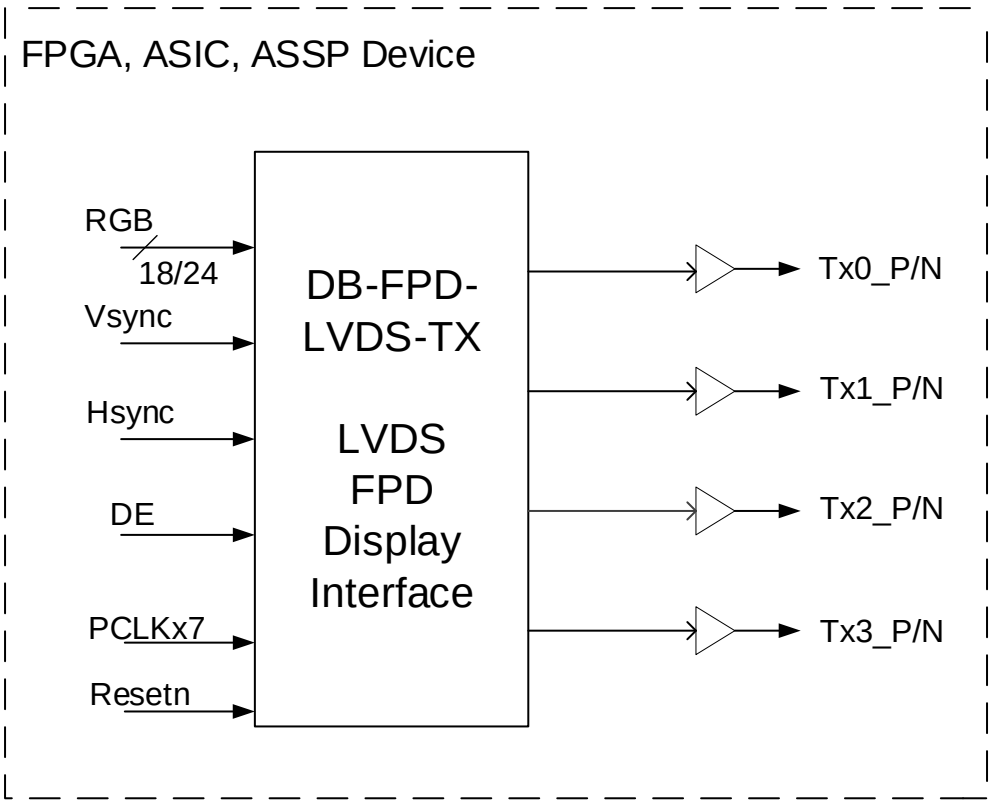

Figure 1: DB-FPD-LVDS-TX Display Interface IP – Top Level Block Diagram

Features

- Supports 3 and 4 data and 1 clock LVDS differential pairs
- 18 / 24 bits-per-pixel (typically RGB or YCbCr)
- Example Range of Video Formats:
  - HD 1280x720p
  - Full HD 1920x1080p
  - Cinema Full HD 2560x1080p
  - UHD 4K x 2K 3840x2160p
- Dual Port LVDS Panel Support Provided
- Supports standardized FPD-Link Panels
- Compatible with commercial LVDS ICs:
  - SN65LVDS*, SN75LVDS*,DS90CR*, DS90UR*, THC63LVD
- Supports 600 Mbps per data pair
- Differential Driver per data pair supplied by user from foundry technology library
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-FPD-LVDS-TX. Please contact Digital Blocks for additional information.

Deliverables

The **DB-FPD-LVDS-TX.** is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with synthesis scripts, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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