General Description

The Digital Blocks DB1845 ITU-R BT.1120 / BT.656 Decoder IP Core decodes ITU-R BT.1120 and BT.656 digital video uncompressed NTSC and PAL video, extracting Y'CbCr 4:2:2 video components and frame timing & status signals. Note that the DB1845 can extract HD 1920x1080 down to SD 720x576/486 images -- and non-standard resolutions in between -- based on programmable settings.

Figure 1 depicts the DB1845 ITU-R BT.1120 / BT.656 Decoder IP Core embedded within an integrated circuit device. Control & Status can be programmed into optional DB1845 registers via a bus interface, or set as non-register fixed parameters at synthesis. Optional Frame and Line Valid input signals enable non-standard image capture and decoder output.

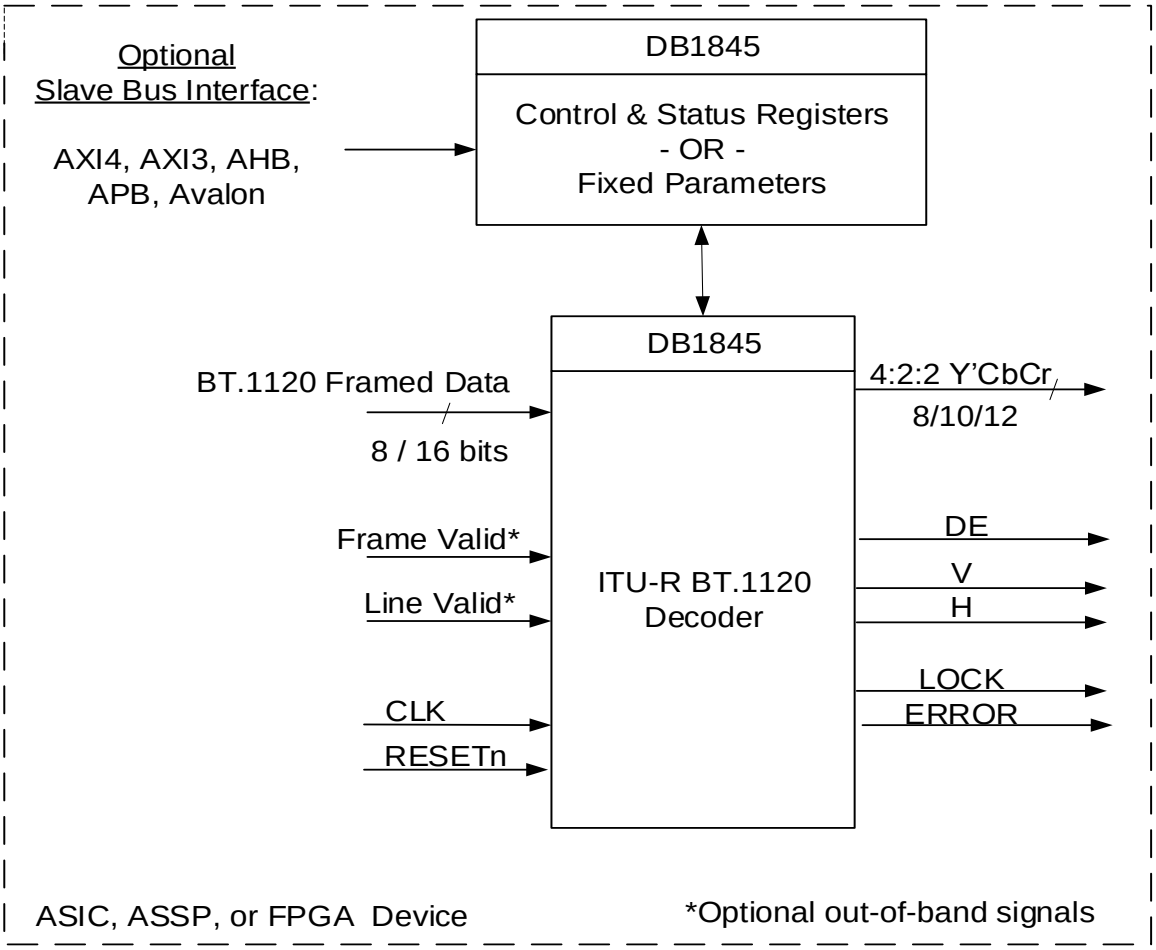

Figure 1: DB1845 ITU-R BT.1120/BT.656 Decoder

Features

- Decodes an ITU-R BT.1120 Frame providing the following outputs:
  - Y'CbCr 4:2:2 color digital components (Luma/Chroma)
  - Data Enable for Luma / Chroma component samples
  - V, H timing synchronization
  - Status - Lock & Error detection
- Programmable 8/10-bit Y'CbCr Symbol extraction
- Supports following High/Standard Definitions:
  - High Definition (HD) – ITU-R BT.1120:
    - NTSC 2200x1100 (1080p/60 Hz)
    - PAL 2640x1320 (1080p/50 Hz)
    - 74.25 / 158.5 MHz
  - Standard Definition (SD) – ITU-R BT.656:
    - NTSC 720x486 (525/60 Video System)
    - PAL 720x576 (625/50 Video System)
    - 27 MHz Sampling Rate
  - Above representative of HD/SD Standards as programming settings and/or incoming Frame determine extracted Y'CbCr Symbols and video timing
- Decodes Interlace & Progressive Images – outputting Progressive Image
- Optional Additional Features:
  - DMA Controller to send decoded Y'CbCr data to memory
  - Color Space Converter – typically to convert to RGB 4:2:2
  - Color Space Converter and Chroma upsampler – to convert to RGB 4:4:4
- User optional Slave Bus Interface for programming Control & Status Registers
- On-Chip Interconnect Compliance (optional) – Avalon/Qsys, AXI, AXI4, AHB:
  - AMBA AXI4 Protocol Specification (V3.0)
  - AMBA AXI3 Protocol Specification (V1.0)
  - AMBA AHB Specification 2.0
  - AMBA APB Specification 2.0
  - Avalon Interface Specification (MNL-AVABUSREF-2.0)
- FPGA Integration Support:
  - Altera Quartus II & Qsys Integration & NIOS II EDS Reference Design
  - Xilinx ISE Design Suite utilizing AMBA AXI4 & Embedded Development & Software Development Kits
- ASIC / ASSP Design-In Support:
  - Compliance to RTL Design & Coding Standards
  - Digital Blocks Support Services
- Fully-synchronous, synthesizable Verilog RTL IP Core, with rising-edge clocking, No gated clocks, and No internal tri-states

Pin Description

DB1845 ITU-R BT.1120 / BT.656 Decoder contains optional AMBA bus AXI4, AXI3, AHB, APB and Avalon bus for processor programming of internal parameters. The DB1845 optionally contains no bus interface with hard-coding of the video transformation parameters.

The DB1845 contains the following I/O interface. For information on a bus fabric interface I/O, please contact Digital Blocks.

Name[2]	I/O Type	I/O Size	Description
Input Interface			
BT1120_CLK	Input	1	BT1120 Pixel Clock (74.25/148.5 MHz)
BT1120_RESETn	Input	1	BT1120 Reset
BT1120_FRAME_DATA[15:0]	Input	8/16	BT1120 Frame Data
BT1120_Frame_Valid[1]	Input	1	BT1120 Frame Valid
BT1120_Line_Valid[1]	Input	1	BT1120 Line Valid
Output Interface			
BT1120_YCRCB_DATA[15:0]	Output	8/16	BT1120 YCbCr Output
BT1120_DE	Output	1	BT1120 Data Enable – Luma/Chroma Components
BT1120_V	Output	1	BT1120 Vertical Sync
BT1120_H	Output	1	BT1120 Horizontal Sync
BT1120_LOCK	Output	1	BT1120 Frame Lock
BT1120_ERROR	Output	1	BT1120 Parity Error Detected

Table 1: DB1845 – I/O Pin Description of ITU-R BT.1120/BT.656 Decoder

[1]Optional Out-of-Band Signals – Used in cases where framing signaling is not within the BT.1120/BT.656 Frame
[2]Though the DB1845 supports ITU-R BT.1120 / BT.656, the Pin Name contains the BT1120 pre-fix, representing the highest standard supported.

Verification Method

The DB1845 contains a test suite with bus functional models that program the DB1845 control & status registers, drives the DB1845 with various standard BT.1120 andBT.656 Frames as well as non-standard Frames with Frame/Line Valid and checks component color data and timing synchronization signal output expected results.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB1845. These include Verilog simulations and encrypted FPGA model. Please contact Digital Blocks for more information.

Deliverables

The DB1845 is available in FPGA netlist or synthesizable RTL Verilog, along with Synopsys Design Constrains, a simulation test bench with expected results, reference design, and user manual.

Support

The DB1845 IP Core is warranted against defects. One year of phone and email technical support is included, starting with the first interaction. Additional maintenance and support options are available.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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