General Description

The Digital Blocks DB1810 Color Space Converter IP Core transforms three color components from one color space to another. An image can be sourced in one color space, while more efficiently processed, stored, or transmitted in another space, while still more effectively displayed in a third color space.

Figure 1 depicts the DB1810 Color Space Converter IP Core embedded within an integrated circuit device. The DB1810 accepts $X_1X_2X_3$ tri-stimulus components and converts them to color space $Y_1Y_2Y_3$ components. Control & Status, including the transforms coefficients, can be programmed into optional DB1810 registers via a bus interface, or set as non-register fixed parameters at synthesis for a smaller VLSI footprint.

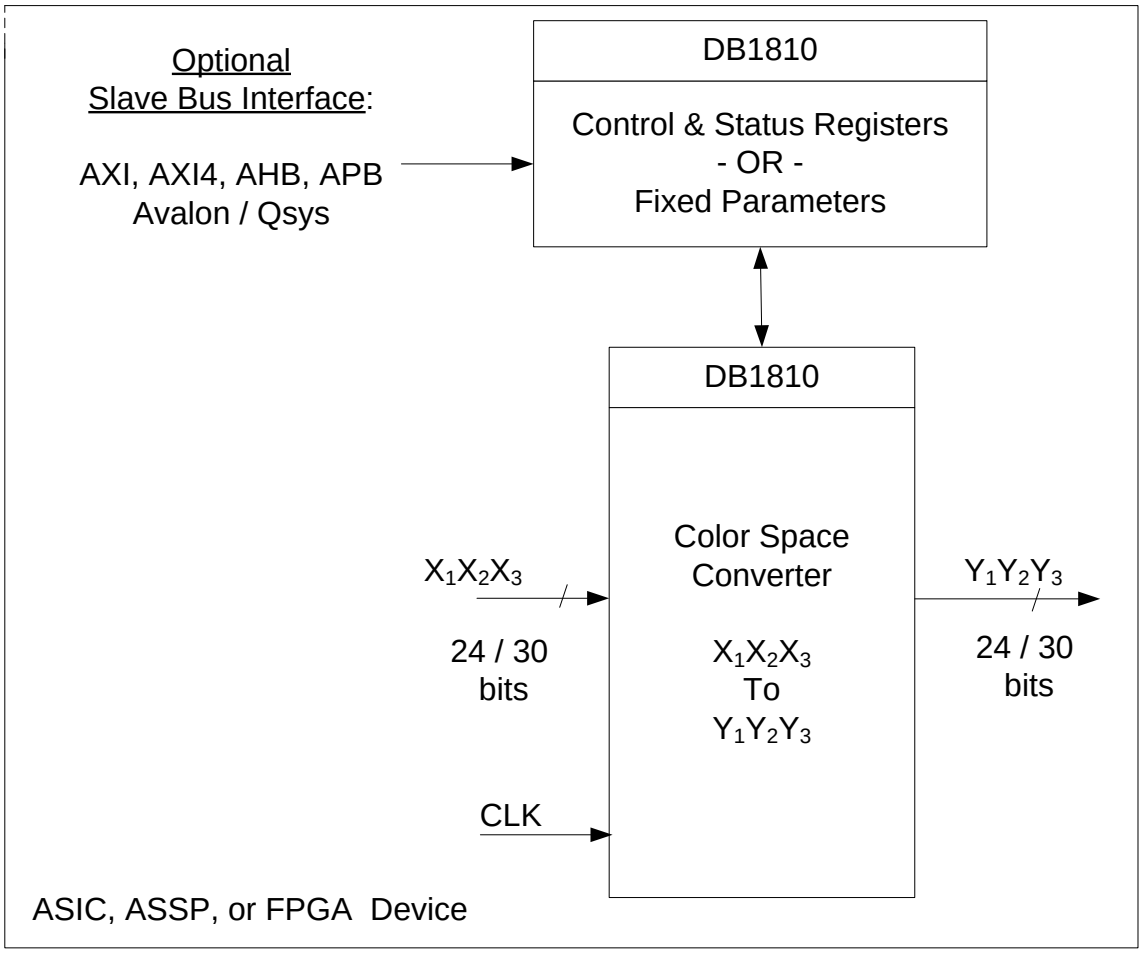

Figure 1: DB1810 Color Space Converter

Color Space Matrix Transform

The DB1810 performs the following 4x4 matrix transform (with summands $S_1S_2S_3$), where $X_1X_2X_3$ represents the input tri-stimulus component samples and $Y_1Y_2Y_3$ the converted output component samples:

$$\begin{bmatrix} C_{11} & C_{12} & C_{13} & S_1 \\ C_{21} & C_{22} & C_{23} & S_2 \\ C_{31} & C_{32} & C_{33} & S_3 \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \\ X_3 \\ 1 \end{bmatrix} = \begin{bmatrix} Y_1 \\ Y_2 \\ Y_3 \end{bmatrix}$$

The DB1810 Color Space Converter can convert between the following standard color spaces. Note that as part of the deliverables, Applications Engineering at Digital Blocks provides the coefficients.

1. Between Computer Display and SD/HD TV:
   - R'G'B' (computer) to Y'CrCb (SD/HD)
   - Y'CrCb (SD/HD) to R'G'B' (computer)

2. Between Studio Computer Display and Studio SD/HD TV:
   - R'G'B' (studio) to Y'CrCb (SD/HD)
   - Y'CrCb (SD/HD) to R'G'B' (studio)

3. Between Computer Display and Full Range Y'CrCb (JPEG/JFIF):
   - R'G'B' (computer) to Y'CrCb (Full Range)
   - Y'CrCb (Full Range) to R'G'B' (computer)

4. Between Y'UV and Computer Display
   - Y'UV to R'G'B'(computer)
   - R'G'B'(computer) to Y'UV

5. Between Computer Display and Y'IQ
   - Y'IQ to R'G'B'(computer)
   - R'G'B'(computer) to Y'IQ

6. User Defined Color Spaces

Features

- $X_1X_2X_3$ and $Y_1Y_2Y_3$ input & output components (for example, $X_1X_2X_3$ = RGB input; $Y_1Y_2Y_3$ = Y'CrCb output) each at 8- or 10-bits, unsigned data type. User selectable at 24- or 30-bit parallel or serial input / output.
- Coefficients are 10-bit signed fractional data type & Summands are 17-bit Signed, integer data type
- After conversion, each $Y_1Y_2Y_3$ sample component can be truncated or rounded-up, and saturated or clamped for overflow or underflow, respectively
- User optional Slave Bus Interface for programming Control & Status Registers, which includes the converters coefficients or fixed parameters set at synthesis
- Member of Digital Blocks' *Video Signal & Image Processing IP Core Family*, which include the following:
    - DB1800 - Standard Definition NTSC/PAL/SECAM Video Sync Separator
    - DB1810 - Color Space Convert
    - DB1820 - Chroma Resampler
    - DB1825 - RGB to YCrCb Color Space Convert with 4:4:4 to 4:2:2 Chroma Resampler
    - DB1830 - BT.656 Encoder
    - DB1840 - BT.656 Decoder
    - DB1892 - RGB to CCIR601/656 Encoder
- On-Chip Interconnect Compliance (optional) – Avalon/Qsys, AXI, AXI4, AHB:
    - Avalon Interface Specification (MNL-AVABUSREF-2.0)
    - AMBA AXI Protocol Specification (V1.0)
    - AMBA AXI4 Protocol Specification (V3.0)
    - AMBA AHB Specification 2.0
    - AMBA APB Specification 2.0
- FPGA Integration Support:
    - Altera Quartus II & Qsys / SOPC Integration & NIOS II EDS Reference Design
    - Xilinx ISE Design Suite utilizing AMBA AXI4 & Embedded Development & Software Development Kits
- ASIC / ASSP Design-In Support:
    - Compliance to RTL Design & Coding Standards
    - Digital Blocks Support Services
- Fully-synchronous, pipelined architecture, synthesizable Verilog RTL core

Pin Description

DB1810 Color Space Converter contains optional AMBA bus AXI, AXI4, AHB, APB and Avalon / Qsys bus for processor programming of internal parameters. The DB1810 optionally contains no bus interface with hard-coding of the video transformation parameters.

The DB1810 contains the following I/O interface. For information on a bus fabric interface I/O, please contact Digital Blocks.

Name	Type	Description
Input Interface		
CSC_PCLK	Input	CSC Sample Clock
CSC_ PRESETN	Input	CSC Reset
CSC_X1	Input	CSC X1 – 1 of 3 Input Color Components
CSC_X2	Input	CSC X2 – 1 of 3 Input Color Components
CSC_X3	Input	CSC X3 – 1 of 3 Input Color Components
CSC_IVLD	Input	CSC Input Valid (Optional)
Output Interface		
CSC_Y1	Output	CSC Y1 – 1 of 3 Output Color Components
CSC_Y2	Output	CSC Y2 – 1 of 3 Output Color Components
CSC_Y3	Output	CSC Y3 – 1 of 3 Output Color Components
CSC_OVLD	Output	CSC Output Valid (Optional)

Table 1: DB1810 – I/O Pin Description of Color Space Converter

Verification Method

The DB1810 contains a test suite with bus functional models that program the DB1810 control & status registers, drives the DB1810 with various standard component color data, and checks expected results.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB1810. These include Verilog simulations, encrypted FPGA models, or the DB1810 Demo System, which includes an Altera FPGA and 320x240 TFT LCD panel.

Deliverables

The DB1810 is available in FPGA netlist or synthesizable RTL Verilog, along with Synopsys Design Constrains, a simulation test bench with expected results, reference design, and user manual.

Support

The DB1810 IP Core is warranted against defects. One year of phone and email technical support is included, starting with the first interaction. Additional maintenance and support options are available.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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