General Description

The Digital Blocks DB9000AXI TFT LCD Controller IP Core interfaces a microprocessor and frame buffer memory via the AMBA AXI Protocol Interconnect to a TFT LCD panel. The DB9000AXI contains a selectable 256 / 128 / 64 / 32-bit AXI Master Interface that targets higher resolution, higher color depth TFT LCD panels, with their resulting high frame buffer memory data bandwidth requirements.

The DB9000AXI IP Core can be implemented in an ASIC, ASSP, or FPGA device with an embedded microprocessor, an AMBA AXI Interconnect fabric, and SDRAM Controller for access to frame buffer memory. Typically, the microprocessor is an ARC, ARM, Intel, MIPS, OpenSPARC, PowerPC, or Tensilica processor and frame buffer memory is off-chip DDR / DDR2 / DDR3 / DDR4 SDRAM.

Figure 1 depicts the system view of the DB9000AXI TFT LCD Controller IP Core embedded within an integrated circuit device.

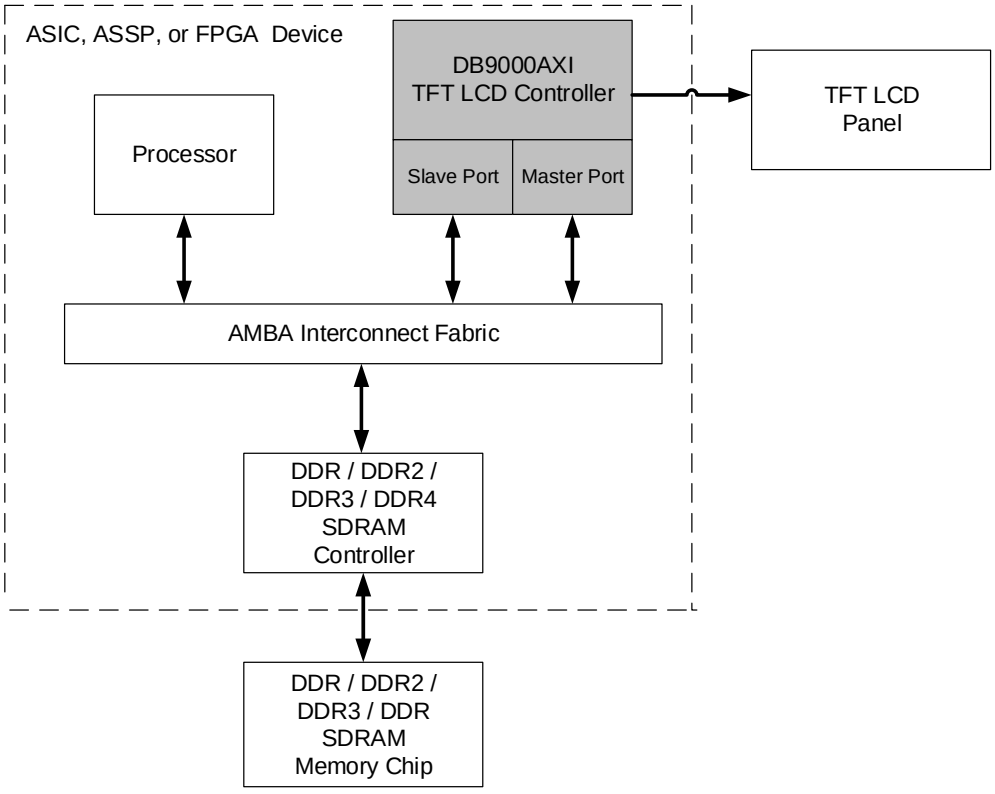

Figure 1: DB9000AXI TFT LCD Controller – System Diagram

Features

- Wide range of programmable LCD Panel resolutions:
  - Maximum programmable resolutions of 8192x8192
  - Horizontal pixel resolutions from 16 to 8192 pixels in 16 pixel increments.
- Example LCD Panel high resolutions:
  - Digital Cinema Systems (DCI) 2048 x 1080 2K image, 4096 x 2160 4K image, & Cinema Scope HD 2560 x 1080
  - 7680x4320, 4096x2560, 3840x2160, 2560x2048, 2048x2048, 2048x1536, 1920x1200, 1920x1080, 1680x1050, 1600x1200
  - 1600x900, 1440x900, 1366x768, 1280x1024, 1280×768, 1080x1920, 1024x768, 1024x600, 1024x576, 960x540, 800x600, 800x480
- Example LCD Panel medium / small resolutions:
  - 640x480, 640x400, 640x240, 640x200, 480x800, 480x640, 480x272
  - 480x234, 240x400, 240x320, 240x240, 320x200, 320x240
- Programmable 1 Port or 2 Port TFT LCD Panel interfaces
- Interface for 1 Port TFT LCD Panel:
  - 18-bit digital (6-bits/color) LVDS / CMOS
  - 24-bit digital (8 bits/color) LVDS / CMOS
- Interface for 2 Port LVDS TFT LCD Panel:
  - Two 24-bit digital (8 bits/color) LVDS / CMOS ports
- Interface to LVDS, DVI, HDMI, & DisplayPort Transmitters / Receivers
- Programmable frame buffer bits-per-pixel (bpp) color depths:
  - 1, 2, 4, 8 bpp mapped through Color Palette to 18-bit LCD pixel
  - 16, 18, bpp directly drive 18-bit LCD pixel
  - 24 bpp directly drive 24-bit LCD pixel
- Color Palette RAM to reduce Frame Buffer memory storage requirements and AXI Bus bandwidth (for lower color applications):
  - 256 entry by 16-bit RAM, implemented as 128 entry by 32-bits
  - Loaded via the Slave Bus Interface statically by the microprocessor or the Master Bus Interface dynamically with each frame by the DMA controller
- Programmable Output format support:
  - RGB 6:6:6 or 5:6:5 or 5:5:5 on 18-bit digital interface
  - RGB 8:8:8 on 24-bit digital interface
- Programmable horizontal timing parameters:
  - horizontal front porch, back porch, sync width, pixels-per-line
  - horizontal sync polarity
- Programmable vertical timing parameters:
  - vertical front porch, back porch, sync width, lines-per-panel

  - vertical sync polarity
- Programmable pixel clock:
  - pixel clock divider from 1 to 128 of Bus Clock
  - pixel clock polarity
- Programmable Data Enable timing signal:
  - Derived from horizontal and vertical timing parameters
  - display enable polarity
- AMBA AXI / AHB / APB Interconnect:
  - Selectable 256 / 128 / 64 / 32-bit AXI Master Port for DB9000AXI DMA access of frame buffer memory for driving the display
  - Selectable 256 / 128 / 64 / 32-bit AXI (or AHB / APB) Slave Port for control & status interface to microprocessor
- Three memories:
  - 32-word x 64 bit input FIFO, decoupling AXI bus & LCD panel clock rates. Integrated with DMA controller.
  - 256-word x 16-bit Color Palette RAM
  - 16-word output FIFO
  - FIFOs parameterizable in depth and width
- Power up and down sequencing support
- 9 sources of internal interrupts with masking control
- Little-endian, big-endian, or Windows CE mode
- AHB / APB Bus - Compliance with AMBA Specification (Rev 2.0)
- AXI Bus - Designed to AMBA AXI Protocol Specification (V1.0)
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, No gated clocks, and No internal tri-states.
- High-Resolution TFT LCD Panel support features by AXI Interconnect / Protocol:
  - Up to 16 overlap outstanding reads requests to the SDRAM Controller
  - Wide AXI Master Port data width, up to 256-bits

Block Diagram

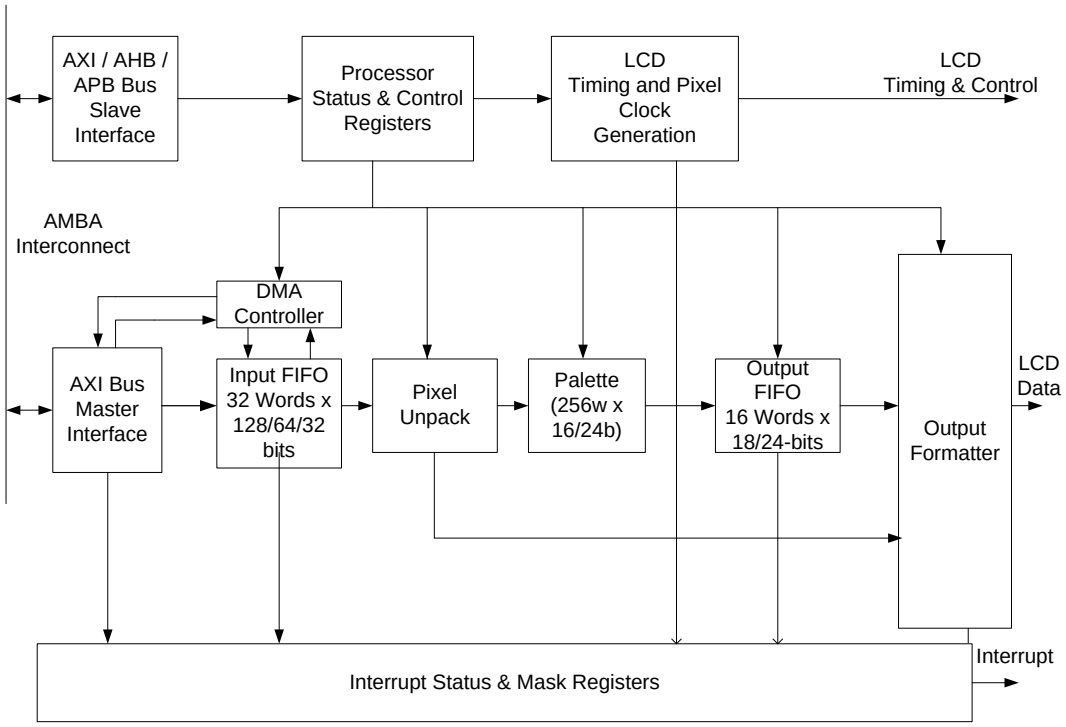

Figure 2: DB9000AXI AMBA Interconnect TFT LCD Controller

Pin Description

The DB9000AXI contains three interfaces:

- LCD Panel Interface
- AMBA AXI Master Interface
- AMBA Slave Interface (optional AXI or AHB or APB)
  (Please Contact Digital Blocks with requirements)

The LCD Interface & AXI Master Interface are listed in Tables 1 & 2 respectively.

Name	I/O Type	Description
LCD Panel Interface – Port 1		
LCD_PCLK	Output	Pixel Clock
LCD_HSYNC	Output	Horizontal Sync Pulse
LCD_VSYNC	Output	Vertical Sync Pulse
LCD_DE	Output	Display Enable
LCD_PE	Output	Power Enable
LCD_R[7:0]	Output	Red Data
LCD_G[7:0]	Output	Green Data
LCD_B[7:0]	Output	Blue Data
LCD Panel Interface – Port 2		
Note: Port 2 shares the common control signals with Port 1: • **LCD_PCLK** • **LCD_HSYNC** • **LCD_VSYNC** • **LCD_DE** • **LCD_PE**		
LCD_R_2[7:0]	Output	Red Data
LCD_G_2[7:0]	Output	Green Data
LCD_B_2[7:0]	Output	Blue Data

Table 1: DB9000AXI – I/O Pin Description for Interface to LCD Panel

Name	I/O	Description
AXI Global Signals		
ARESETn	I	**Reset** – Active LOW Reset for AXI Master and DB9000 core.
ACLK	I	**Bus Clock** – Clock for AXI Master and one of two programmable clock sources generating PCLK. All AXI Master logic, including DMA Controller and ingress part of Input FIFO triggered on ACLK rising edge.
AXI Read Address Channel Signals		
ARID[3:0]	O	**Read Address ID**
ARADDR[31:0]	O	**Read Address Bus -** Address bus to the AXI Bus for reading of Frame Buffer Memory.
ARLEN[3:0]	O	**Burst Length** – Indicates number of word transfers in a burst. DB9000 AXI Master supports 1, 4, 8, 16 word transfers.
ARSIZE[2:0]	O	**Transfer Size** – Indicates the size of the transfer. DB9000 supports only word (8bytes/64-bit) transfer sizes.
ARBURST[1:0]	O	**Burst Type** – Burst Type, coupled with size information, details how address for each transfer within burst is calculated. DB9000 supports only burst type INCR – Incrementing Burst Type.
ARLOCKM	-	**Locked Type** – Unused by DB9000.
ARCACHE[3:0]	-	**Cache Type** – Unused by DB9000.
ARPROT[2:0]	-	**Protection Type** – Unused by DB9000.
ARVALID	O	**Read Address Valid –** When asserted HIGH indicates read address and control information valid on AXI bus.
ARREADY	I	**Read Address Ready –** When HIGH indicates Slave ready to accept address and associated control information.
AXI Read Data Channel Signals		
RID[3:0]	I	**Read ID Tag**
RDATA[63:0]	I	**Read Data Bus -** Contains read data from Frame Buffer Memory.
RRESP[1:0]	I	**Read Response –** Provides additional information on the status of a transfer.
RLAST	I	**Read Last –** Indicates the last transfer in a read burst.
RVALID	I	**Read Valid** – HIGH indicates required read data available and DB9000 can accept the data word.
RREADY	O	**Read Ready** – HIGH indicates the DB9000 can accept read data and response information.

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Table 2: DB9000AXI – I/O Pin Description for Interface to AXI Master Bus

Verification Method

The DB9000AXI contains a simulation test suite with AXI Bus functional models that program the DB9000AXI control & status registers via the AXI/AHB/APB Slave Bus, generates frame buffer data in response to AXI Master requests, and checks expected results.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB9000AXI. Please contact Digital Blocks for additional information.

Deliverables

The DB9000AXI is available in synthesizable RTL Verilog, along with a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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