General Description

The Digital Blocks DB9000AHB TFT LCD Controller IP Core interfaces a microprocessor and frame buffer memory via the AMBA 2.0 AHB Bus to a TFT LCD panel. In an FPGA, ASIC, or ASSP device, the microprocessor is an ARM processor and frame buffer memory is either on-chip SRAM memory or larger off-chip SRAM or SDRAM. Figure 1 depicts the system view of the DB9000AHB TFT LCD Controller IP Core embedded within an integrated circuit device.

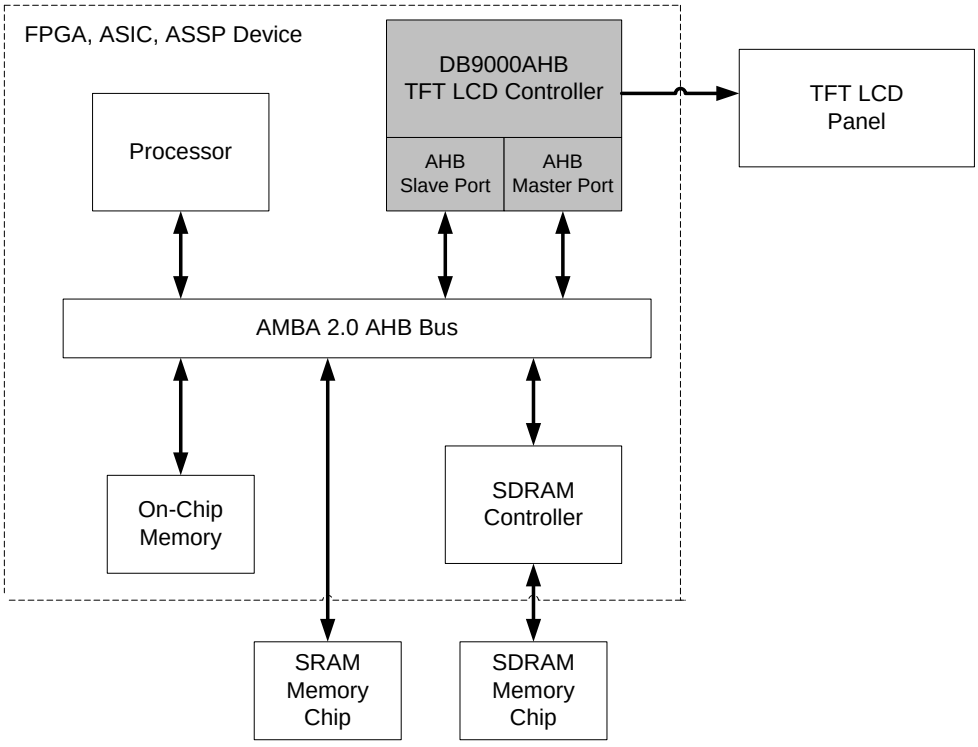

Figure 1: DB9000AHB TFT LCD Controller – System Diagram

Features

- Wide range of programmable LCD Panel resolutions:
  - Maximum programmable resolutions of 4096x4096
  - Horizontal pixel resolutions from 16 to 4096 pixels in 16 pixel increments.
- Example LCD Panel high resolutions:
  - 4096x2560, 3840x2160, 2560x2048, 2048x2048, 2048x1536, 1920x1200, 1920x1080, 1680x1050, 1600x1200
  - 1600x900, 1440x900, 1366x768, 1280x1024, 1280×768, 1080x1920, 1024x768, 1024x600, 1024x576, 960x540, 800x600, 800x480
- Example LCD Panel medium / small resolutions:
  - 640x480, 640x400, 640x240, 640x200, 480x800, 480x640, 480x272
  - 480x234, 240x400, 240x320, 240x240, 320x200, 320x240
- Support for 1 Port TFT LCD Panel interfaces:
  - 18-bit digital (6-bits/color) & 24-bit digital (8-bits/color)
- Programmable frame buffer bits-per-pixel (bpp) color depths:
  - 1, 2, 4, 8 bpp mapped through Color Palette to 18-bit LCD pixel
  - 16, 18, bpp directly drive 18-bit LCD pixel
  - 24 bpp directly drive 24-bit LCD pixel
- Color Palette RAM to reduce Frame Buffer memory storage requirements and AHB Bus bandwidth:
  - 256 entry by 16-bit RAM, implemented as 128 entry by 32-bits
  - Loaded via the Slave Bus Interface statically by the microprocessor or the Master Bus Interface dynamically with each frame by the DMA controller
- Programmable Output format support:
  - RGB 6:6:6 or 5:6:5 or 5:5:5 on 18-bit digital interface
  - RGB 8:8:8 on 24-bit digital interface
- Programmable horizontal timing parameters:
  - horizontal front porch, back porch, sync width, pixels-per-line
  - horizontal sync polarity
- Programmable vertical timing parameters:
  - vertical front porch, back porch, sync width, lines-per-panel
  - vertical sync polarity
- Programmable pixel clock:
  - pixel clock divider from 1 to 128 of Bus Clock
  - pixel clock polarity
- Programmable Data Enable timing signal:
  - Derived from horizontal and vertical timing parameters
  - display enable polarity

- Three memories:
    - 16-word x 32 bit input FIFO, decoupling AHB bus & LCD panel clock rates. Integrated with DMA controller.
    - 256-word x 16-bit Color Palette RAM
    - 16-word output FIFO
    - FIFOs parameterizable in depth and width
- Power up and down sequencing support
- 9 sources of internal interrupts with masking control
- Little-endian, big-endian, or Windows CE mode
- Compliance with AMBA Specification (Rev 2.0)
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, No gated clocks, and No internal tri-states.

Block Diagram

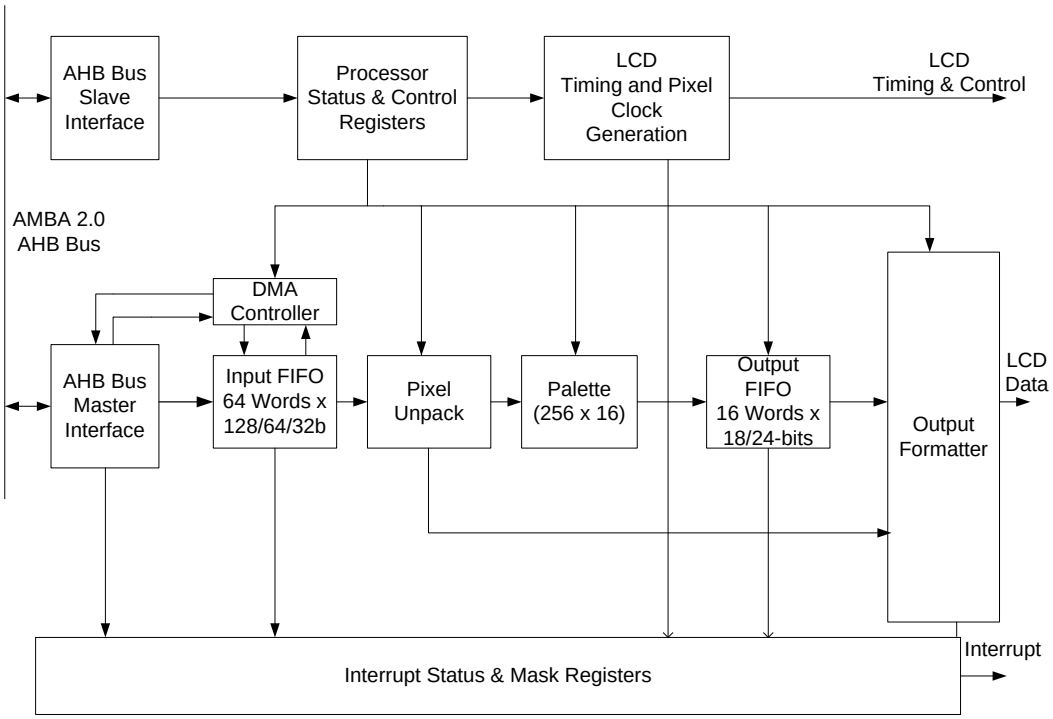

Figure 2: DB9000AHB AMBA 2.0 AHB Bus TFT LCD Controller

Pin Description

In addition to the AMBA 2.0 AHB Master and Slave Bus interfaces, which include the input HCLK and HRESETN signals and the output INTR (interrupt) signal, the interface to the LCD panel is listed in Table 1. Note that if the panel is 18-bits data, the lower 6-bits of LCD_R, LCD_G, and LCD_B should be connected.

Name	Type	Description
LCD Panel Interface		
LCD_PCLK	Output	Pixel Clock
LCD_HSYNC	Output	Horizontal Sync Pulse
LCD_VSYNC	Output	Vertical Sync Pulse
LCD_DE	Output	Display Enable
LCD_PE	Output	Power Enable
LCD_R[7:0]	Output	Red Data
LCD_G[7:0]	Output	Green Data
LCD_B[7:0]	Output	Blue Data

Table 1: DB9000AHB – I/O Pin Description for Interface to LCD Panel

Verification Method

The DB9000AHB contains a test suite with AHB Bus functional models that program the DB9000AHB control & status registers, generates frame buffer data in response AHB Master requests, and checks expected results.

The DB9000AHB IP Core has been verified in an FPGA, driving a variety of TFT LCD panels, including NEC & Sharp 320x240, 480x272, 640x480, 800x600, and 1280x768 resolution panels with an 18-bit or 24-bit digital interface.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB9000AHB. Please contact Digital Blocks for additional information.

Deliverables

The DB9000AHB is available in technology-specific netlists for FPGAs or synthesizable RTL Verilog, along with synthesis scripts, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

Digital Blocks, Inc.
PO Box 192
587 Rock Rd
Glen Rock, NJ 07452 USA
Phone: +1-201-251-1281
eFax: +1-702-552-1905
info@digitalblocks.com

Copyright © Digital Blocks, Inc. 2007-2016, ALL RIGHTS RESERVED

###
Digital Blocks is a registered trademark of Digital Blocks, Inc.
ARM and AMBA are registered trademarks of ARM Limited.