General Description

The Digital Blocks DB9200AXI4 2D Graphics Hardware Accelerator / Engine Verilog IP Core renders graphics frames as follows:

- Generates bitmaps from graphics instructions as well as combining existing bitmaps on and off-screen using one of 256 Raster Operations. A Raster Operation (ROP) is a bitwise Boolean operation (such as AND, OR, XOR, NOT) which lay the foundation for power hardware graphics primitive operations
- Generates characters from compressed bitmaps using its FONT Bitmap Color Expansion Unit
- Performs Alpha Blend operations of bitmaps with its Alpha Blend unit
- Draws lines, polygons, circles using its hardware efficient & pixel accurate Bresenham Algorithm Line Drawing Unit

The DB9200 2D Graphics Hardware Engine provides options for higher graphics performance as a Graphics Processing Unit (GPU) as follows:

- Display List Processing Unit - reads in the graphics instructions for execution
- Parallel Pixel Processing - as wide as the AXI4 Interconnect Data
- Memory Interface Units - with DMA Controller that can burst in and out pixels, helping to unlock the graphics memory bottleneck.

Figure 1 depicts the system view of the DB9200AXI4 2D Graphics Engine Verilog IP Core embedded within an ASIC, ASSP, or FPGA component. Optionally the DB9000 TFT LCD Controller IP Core is depicted as the Display Controller driving the display.

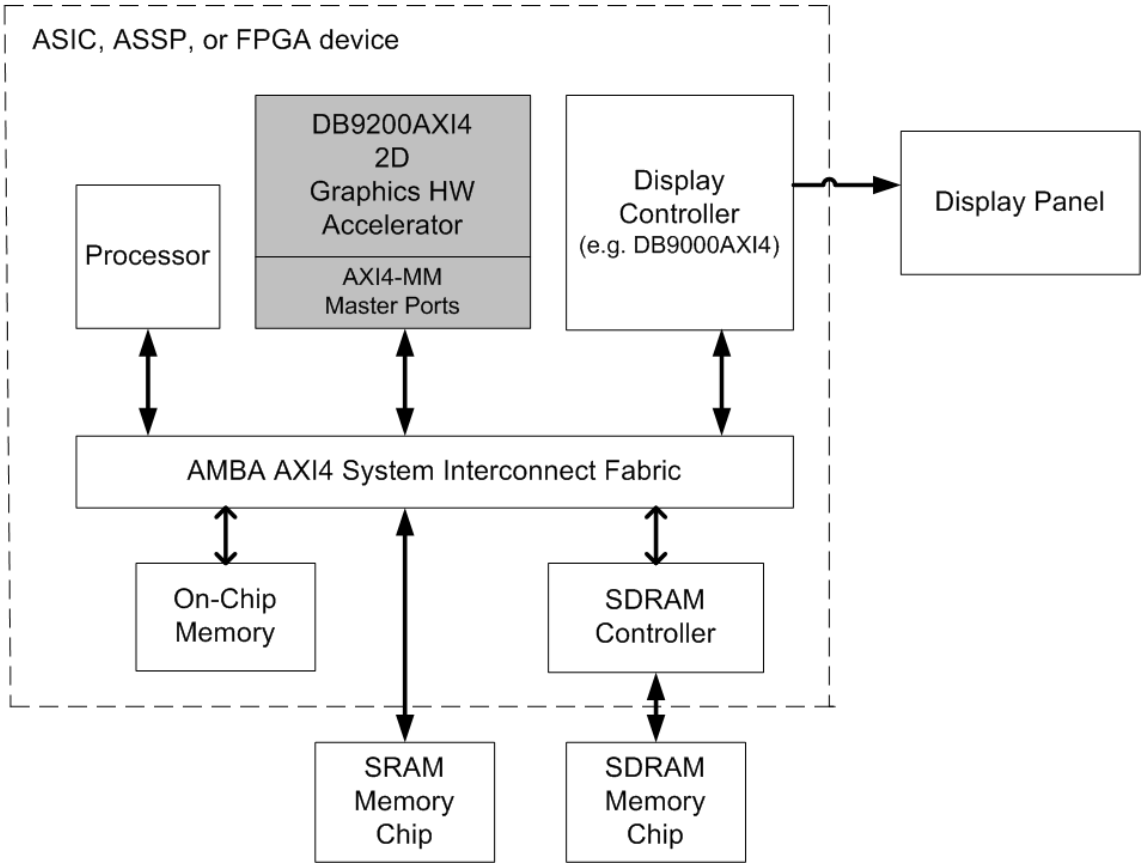

Figure 1: DB9200AXI 2D Graphics Hardware Accelerator – System Diagram

Features

- Bit Block Transfer – 3 Independent Memory Sources of data:
  - On-Screen & Off-Screen Data Block (SRC)
  - Off-Screen Fixed Pattern Data Block (PTN)
  - On-Screen visible Data Block (DST)
- Raster Operations (ROP) performed on Block Transfers:
  - 256 Raster Operations
  - ROP0, ROP1, ROP2, & ROP3 operations
  - Includes industries most popular 16 ROPs
- BitBLT Draw Features:
  - Pixels, Horizontal & Vertical Lines
  - Overlapping & Non-Overlapping Block Transfers
  - Solid Color Block Fills
  - FONT Monochrome Bitmap to Color Expansion, either Transparent or Opaque
  - Rotation Block Transfers: 0, 90, 180, 270 degrees
  - Block Stretch on X & Y Axis
  - Alpha Blending
  - Sprite Moves
- Line Draw Graphics Operations:
  - Pixel Draw
  - Line (Vector) Draw
  - Poly Line Draw (up to 16 segments)
  - Circle Draw
  - Ellipse - (Option – Please contact Digital Blocks)
- Command FIFO or Link-List Display Processing Unit:
  - Simplifies Processor Interface
  - Minimizes Processor Overhead
- Frame Buffer & Display Features Supported:
  - Display Resolutions 4K x 4K
  - 4 GB Memory Range
  - 8, 16 , 24, & 32 bits-per-pixel color depths
- Interrupt Controller with 3 sources of internal interrupts with masking control
- Reference Software Driver Included
  - Reference Driver
  - Graphics API Reference Design
- On-Chip Interconnect Compliance - AXI4:
  - AMBA AXI4 Protocol Specification (V3.0)
- FPGA Integration Support:

  - Altera Quartus II & Qsys Integration & ARM / NIOS II EDS Reference Design
  - Xilinx Vivado IP Integrator & Reference Design
- ASIC / ASSP Design-In Support:
  - Compliance to RTL Design, Coding, & Verification Standards
  - Digital Blocks Support Services
- Compatible with optional Digital Blocks DB9000 Family of TFT LCD Controller IP Cores and Reference Designs
- Fully-synchronous, synthesizable Verilog RTL core.

Deliverables

The DB9200AXI4 is available in RTL Verilog, along with synthesis scripts, a simulation test bench with expected results, reference design, datasheet, and user manual.

Support

The DB9200AXI4 IP Core is warranted against defects for three years. One year of phone and email technical support is included, starting with the first interaction. Additional maintenance and support options are available.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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