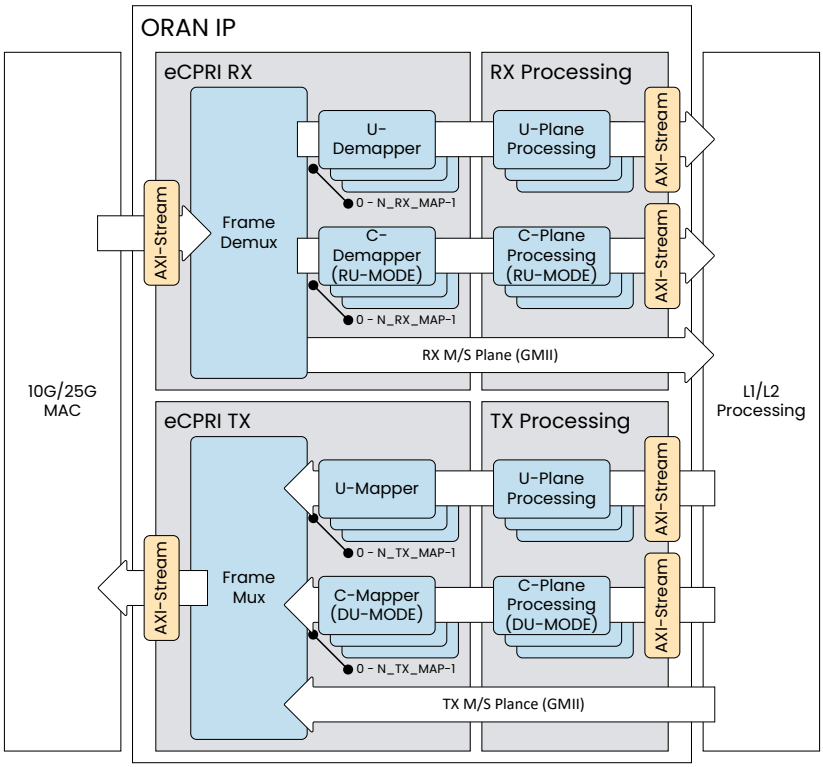
Overview

Chip Interfaces ORAN IP core is a highly scalable and silicon agnostic implementation of the interoperable O-RAN WG4 defined 7.2x interface for deployment in O-DU and O-RU products, targeting any ASIC, FPGA or ASSP technologies. The ORAN over eCPRI implementation builds on long-time experience designing CPRI and Radio-Over-Ethernet solutions for fronthaul and delivers a flexible engine that is prepared for tight integration with software applications.

The IP is designed to meet or exceed the requirements of radio systems, base band systems, fronthaul switches or advanced test systems. The speed optimized core can handle any solutions reaching from the "small footprint" to the most complex applications running 25 Gbps. The IP can dynamically be configured to handle wireless multi-mode radio systems enabling high-performance throughputs required by 4G and 5G wireless solutions.



Key Features

Richly Featured	Support for frequency-domain IQ transport Supports 10G/25G Ethernet MAC ports O-RU and O-DU variants available Multiple Section Extension Types Supported Wide flexibility for configuring
Easy to use	Testbench with typical system configuration and examples
Silicon Agnostic	Designed in HDL and targeting any RTL implementation like ASICs, ASSPs and FPGAs
Highly Configurable	Supporting small to large system configurations

Specification

Feature	Availability	Comment
General Features		
Supports O-RAN CUS-plane 3.0 specification	Yes	
Supported functional split	7-2x	
Technology	System Verilog	
Supported Message Types	0, 2, 5	eCPRI: 0 - IQ, 2 - RealTime, 5 -Delay packets
Supported Section Types	0, 1, 3	
Supported Section Extension Types	6, 10, 11	
Programmable static-bit-width Fixed Point IQ	16 bit	
Compressed IQ Block floating point compression	(7), 9, 12, 14	
Static configuration of U-Plane IQ format and compression header	Yes	configured by register
Supports for lls-du timing advance (Fixed timing advance, dynamic timing advance)	Yes	
Reception window monitoring (counters for Rx_on_time / Rx_early / Rx_late / Rx_corrupt / Total_msgs_recived)	Yes	Event counters per flow - C/U-Plane
QoS over Fronthaul	Yes	VLAN tagging
Support for 10G and 25G Ethernet traffic in RX/TX	Yes	
Number of Ethernet ports supported for aggregation of traffic	1-4	
Support filtering of inbound Ethernet traffic based on MAC and packet headers	Yes	
Support application fragmentation	Yes	Multisection and Section_ID
Support of jumbo frames with up to 9000 bytes of MTU payload	Yes	
Synchronization		
Timing reference	ToD counter	
AxC transmission/reception transmission trigger.	ToD or PPS input	Each flow can be initiated with a different value/source.
ToD bus width	80-bit	
Ethernet Interface		
Number of Ethernet ports towards network transport layer	1	
Ethernet MAC interface standard	Avalon streaming AXI-S	

Specification

Feature	Availability	Comment
CPU Interface		
Internal register width	32 bits	
IRQ support	Yes	
Interface standards supported	Avalon AXI4-Lite APB	
Clock and Reset		
IP main clock frequency	Up to 390.625 MHz	
IP CPU register clock frequency	100 MHz	
IP Ethernet interface clock frequency towards Ethernet MAC	156.25/390.625	
Separate resets for RX, TX and Register interface	Yes	
Deliverables		
Code	SystemVerilog	
Documentation	Yes	
Simulation Environment	Yes	
Programming register specification	Yes	
Timing Constraints in Synopsys SDC format	Yes	
Access to Support System	Yes	
Synopsys SGDC Files	Yes	
Synopsys Lint, CDC and Waivers	Yes	

Ordering Info

Delivery Option code	Delivery Option Code
B	RTL Source Code
D	Encrypted RTL

Technology code	Target Technology
A	ASIC
F	FPGA

Model code	Model description
01	ORAN IP