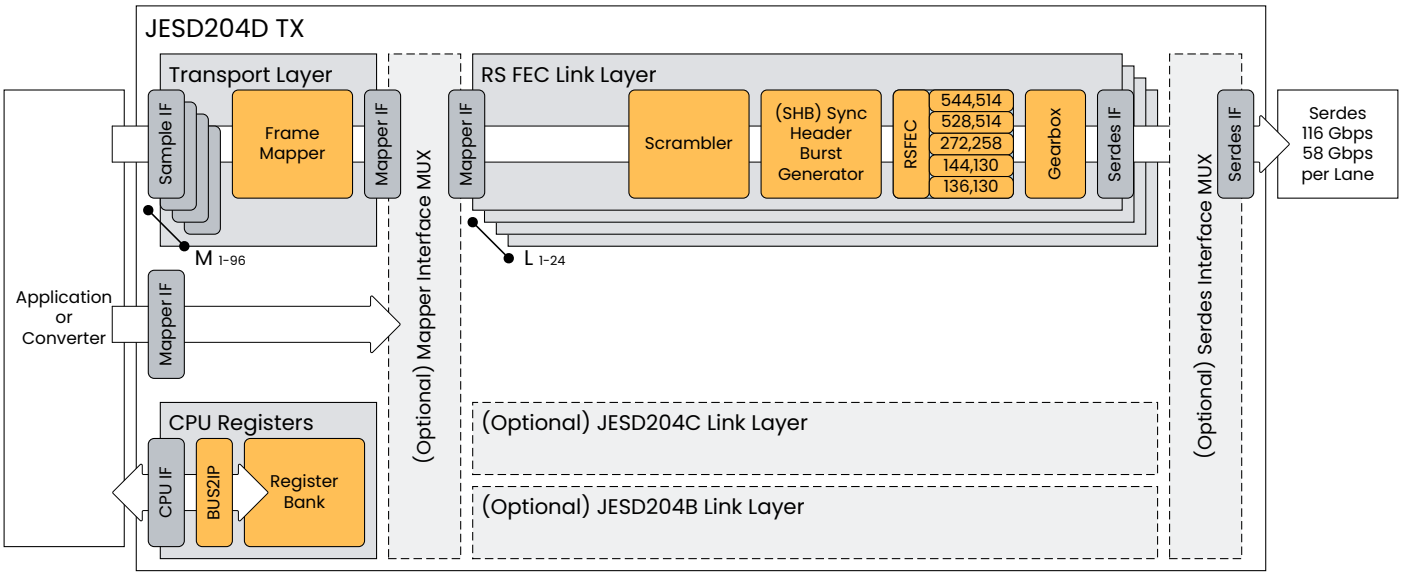
JESD204D IP Core

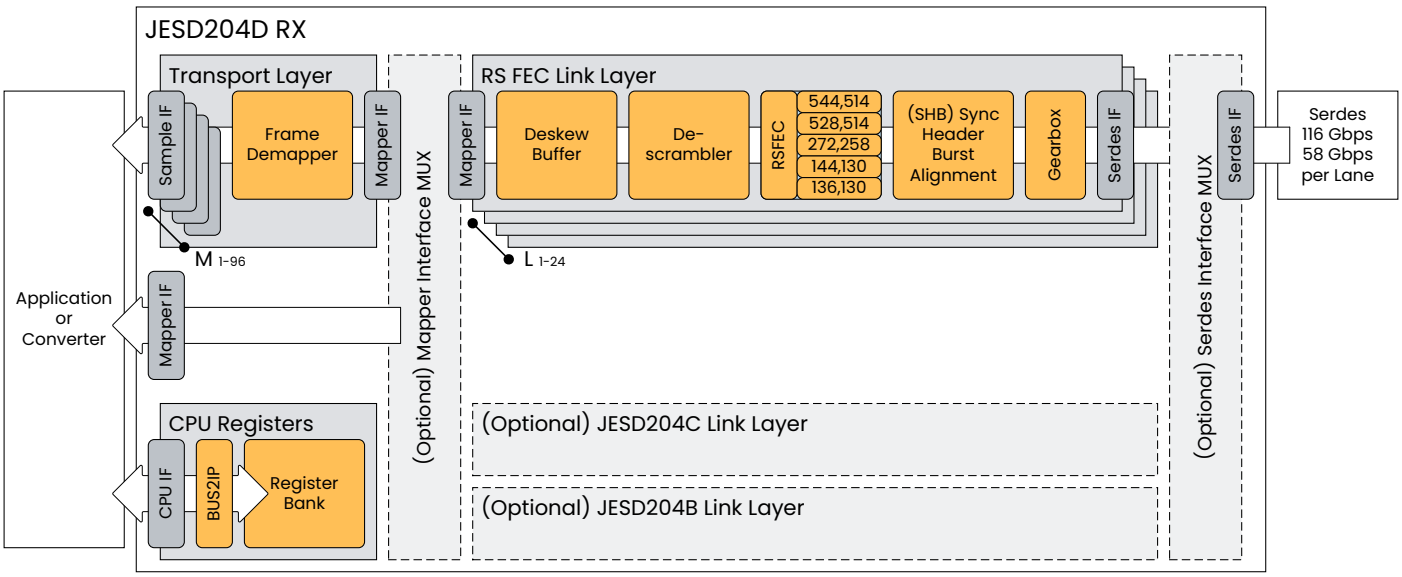
Datasheet V. 1.0 - July 2025

Overview

The JESD204D Controller IP from Chip Interfaces is based on the recently released D revision of the JEDEC standard for Serial Interface for Data Converters. The JESD204D IP core supports line speeds up to 116Gbps with PAM4 and 58Gbps with NRZ and includes full backwards compatibility with 32.5 Gbps JESD204C.1 64b 66b link layer and 16 Gbps JESD204B 8b 10b link layer.

The IP core enables quick and reliable deployment of the transmitter (TX), the receiver (RX) link layer and comes optionally with a tightly integrated transport layer option, that can dynamically be configured to handle any Multiple-Converter Device Alignment, Multiple Lanes (MCDA-ML) requirements. The IP comes with the widest parameter set available and has gone through extensive testing. The IP core is heavily tested in UVM regression environment.





Key Features

Richly Featured	Line rates up to 116 Gbps, supports 1-24 lanes and 1-96 converters Performs standard required scrambling Supports Subclasses (0, 1 and 3) RS-FEC (544,514), RS-FEC (528,514), RS-FEC (272,258), RS-FEC (144,130) and RS-FEC (136,130)
Solid	Silicon proven Lint/CDC optimized UVM regression tested with full coverage Interoperability tested with leading PHY/SerDes/ADC/DAC vendors
Easy to use	Solid documentation including integration guide Easy to use RTL test environment Strong engineering support for bring-up
Silicon Agnostic	Targeting both ASICs and FPGAs

Specification

Feature	Performance/Availability	Comment
General Features		
Standards	JEDEC JESD204D	December 2023
Features Supported	a, b, c, d, e, f, g, h, i	(Table 12 in standard)
Technology	Verilog/System Verilog	For ASIC and FPGA
Line Rates	Up to 116 Gbps	
Lanes (L)	1-24	Runtime Configurable
Number of converters (M)	1-96	Runtime Configurable
Frame Size (F)	1-96	Runtime Configurable
Converter Samples per frame (S)	1-8	Runtime Configurable
Sample Widths (N)	8-32	Runtime Configurable
Total number of bits per sample in the user data format (N')	8, 12, 16, 20, 24, 28, 32	Runtime Configurable
Control bits per sample (CS)	0-3	Runtime Configurable
Control Words (CF)	0-1	Runtime Configurable
HD mode	0-1	Runtime Configurable
Configuration	APB	
	AXI4-Lite / Avalon	
Mandatory Test Sequences	PRBS test patterns	
Debug	Yes	Debug signals can be provided
Test features	TL - Short Test Pattern Long Test Pattern	Runtime Configurable
RS-FEC Encoding		
Payloads in Alignment Block (A)	1-32	Runtime Configurable
Subclasses	0, 1, 3	Runtime Configurable

Feature	Performance/Availability	Comment
Receiver/Transmitter		
FEC1 RS(136,130)	On-Request	Configurable via define, runtime selectable
FEC2 RS(144,130)	On-Request	
FEC3 RS(272,258)	Yes	
FEC4 RS(544,514)	Yes	
FEC5 RS(528,514)	On-Request	
RS-FEC Error Detection Only	Yes	Configurable via define, enabled for PAM2/NRZ
RS-FEC Internal Data width	256 bit, 128 bit, 64 bit	Selectable at complie time
Scrambling	Yes	
Gearbox	Yes	
Interfaces		
Data interface (with mapper)	Data (MxSonIxN) Control bits (MxSonIx3)	Depends on the number of Converters (M) and Number of Samples on Interface (SonI) and bits per sample (N)
Samples on Interface (SonI)	1-8	
Data interface (no mapper)	256 bits per lane	Xilinx AXI4-stream compliant
SerDes interface	10-160 bits per lane	
CPU Interface	32 bits	APB / AXI4-lite / Avalon
Deliverables		
Code	SystemVerilog	Source code or Encrypted RTL
Documentation	Yes	Including User Manual, Release Note and Quick Start Guide
Simulation Environment	Yes	Simple Test Environment, Test Cases, Test Scripts
Timing Constraints in Synopsys SDC Format	Yes	
Access to Support System	Yes	
Synopsys SGDC Files	Yes	
Synopsys Lint, CDC and Waivers	Yes	
Verification report	Yes	
Items available for purchase		
SystemVerilog UVM VIP	Yes	Encrypted

Size Estimates

Size estimates depend on generic settings and compile time parameter. Estimates for ASIC and FPGA are available on request and under NDA. Please contact sales@chipinterfaces.com for more information.

Ordering Info

Delivery Option code	Delivery Option
B	RTL Source Code
D	Encrypted RTL

* Encryption method supported in Cadence and Synopsis. Other can be supported on request

Technology code	Target Technology
A	ASIC
F	FPGA

Model code	Model description
IP core	
01	JESD204D RX Link layer
02	JESD204D RX Link and transport layer
03	JESD204D TX Link layer
04	JESD204D TX Link and transport layer
05	JESD204D RX + TX Link layer
06	JESD204D All
Verification Component	
CV_JESD204D_01	JESD204D UVM VIP (Encrypted SystemVerilog)