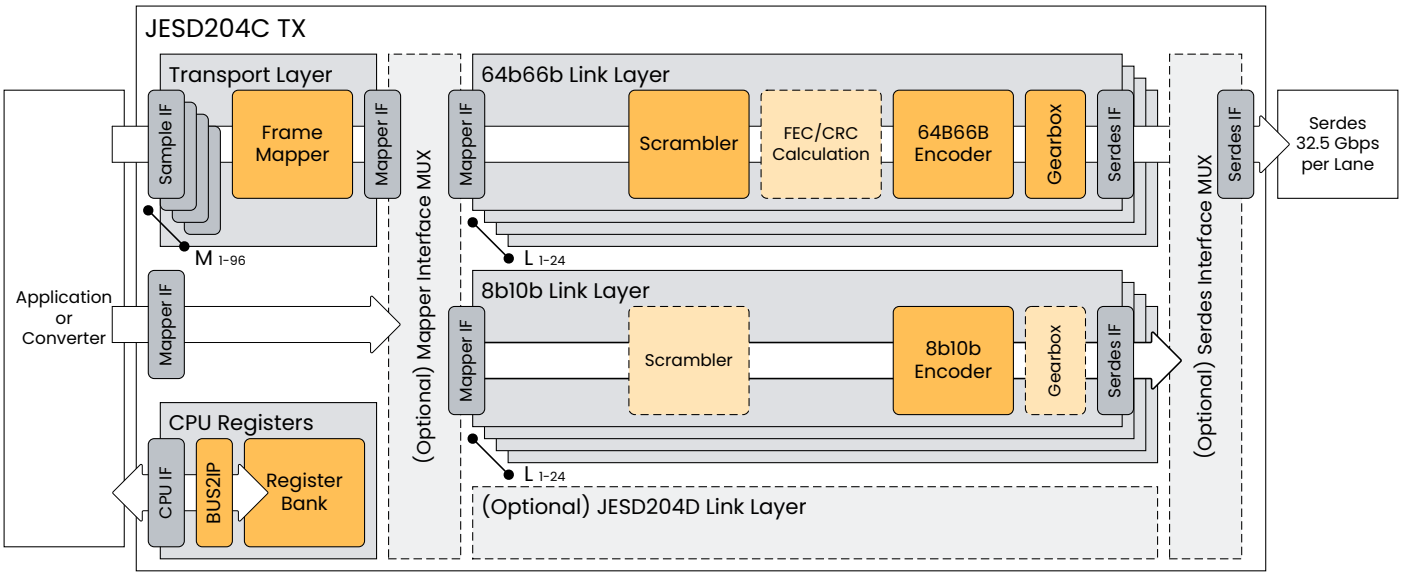
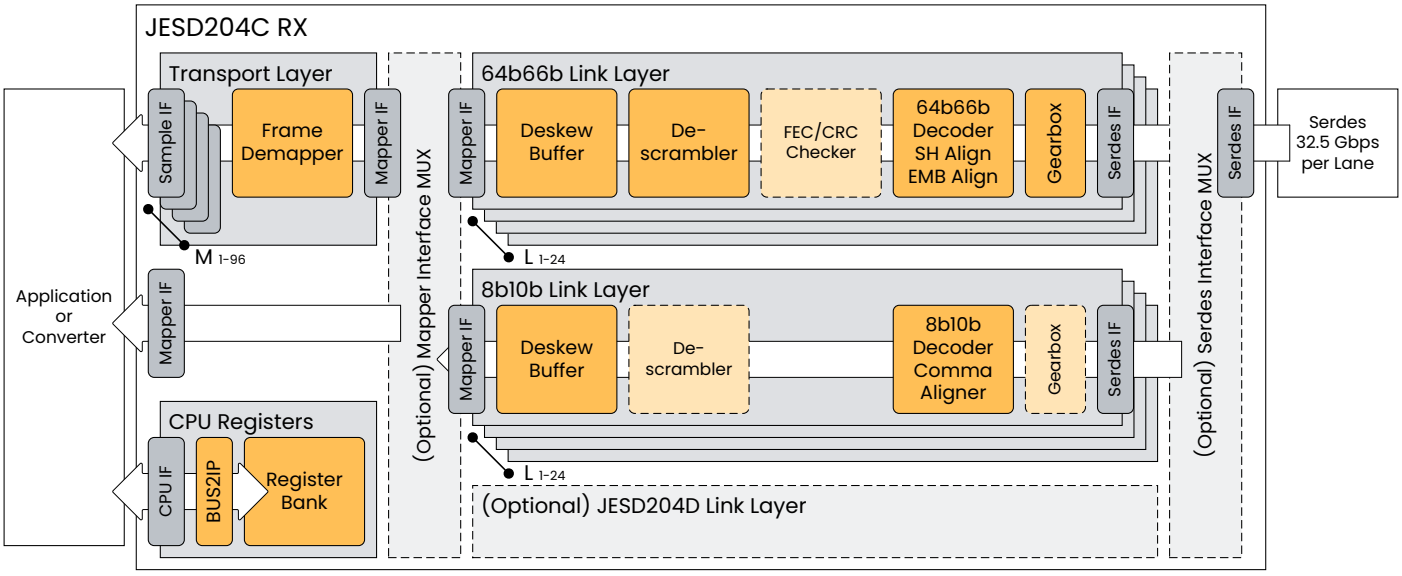
JESD204C IP Core

Datasheet V. 1.0 - July 2025

Overview

The JESD204C controller IP is a highly optimized and silicon agnostic implementation of the JEDEC JESD204C.1 standard serial interface targeting both ASICs and FPGAs. The IP core supports line speeds up to 32.5 Gbps per lane and includes full backwards compatibility with JESD204B and its 8b10b encoding. The IP core enables quick and reliable deployment of the transmitter (TX), the receiver (RX) link layer and comes optionally with a tightly integrated transport layer option, that can dynamically be configured to handle any Multiple-Converter Device Alignment, Multiple Lanes (MCDA-ML) requirements. The IP comes with the widest parameter set available and has gone through extensive testing. The IP core is silicon proven, heavily tested in UVM regression environment and has been interoperability tested with key ADC/DAC providers and leading SerDes PHY solutions.





Key Features

Richly Featured	Link and transport layer available 8b10b, 64b66b, 64b80b encoding/decoding supported Scrambling and de-scrambling included Support for all subclasses (0, 1, 2)
Solid	Silicon proven Lint/CDC optimized UVM regression tested with full coverage Interoperability tested with leading PHY/SerDes/ADC/DAC vendors
Easy to use	Solid documentation including integration guide Easy to use System Verilog Testbench Strong engineering support for integration and bring-up
Silicon Agnostic	Targeting both ASICs and FPGAs

Specification

Feature	Performance/Availability	Comment
General Features		
Standards	JEDEC JESD204C.1	December 2021
Features Supported	a, b, c, d, e, f, g, h, i, j, k, l, m, n	(Table 13 in standard)
Technology	Verilog/System Verilog	For ASIC and FPGA
Line Rates	Up to 32.5 Gbps	
Lanes (L)	1-24	Runtime Configurable
Number of converters (M)	1-96	Runtime Configurable
Frame Size (F)	1-96	Runtime Configurable
Converter Samples per frame (S)	1-8	Runtime Configurable
Sample Widths (N)	8-32	Runtime Configurable
Total number of bits per sample in the user data format (N')	8, 12, 16, 20, 24, 28, 32	Runtime Configurable
Control bits per sample (CS)	0-3	Runtime Configurable
Control Words (CF)	0-1	Runtime Configurable
HD mode	0-1	Runtime Configurable
Mandatory Test Sequences	Supported	
Debug	Yes	Debug signals can be provided
Test features	LL_8b10b - continuous K28.5, Repeated ILAS, Continuous D21.5, 50 Octet JSPAT, JTSPAT, PRBS15 and Continuous Low Freq Pattern	Runtime Configurable
	TL - Short Test Pattern Long Test Pattern	
64b66b/64b80b		
Extended Multiblock Size (E)	1-128	Runtime Configurable
Subclasses	0, 1	Runtime Configurable

Feature	Performance/Availability	Comment
8b10b		
Multi frame (K)	1-256	Runtime Configurable
Subclasses	0, 1, 2	Runtime Configurable
Receiver/Transmitter		
PCS (8b10b coding)	Yes	Can optionally be bypassed
PCS (64b66b coding)	Yes	Can optionally be bypassed
PCS (64b80b coding)	Yes	Can optionally be bypassed
CRC12	Yes	Can optionally be bypassed
CRC3	Yes	Can optionally be bypassed
CMDC	Yes	Can optionally be bypassed
Firecode FEC	Yes	Can optionally be bypassed
Scrambling	Yes	Can optionally be bypassed
Gearbox	Yes	
Interfaces		
Data interface (with mapper)	Data (MxSonIxN) Control Bits (MxSonIx3)	Depends on the number of Converters (M) and Number of Samples on Interface (SonI) and bits per sample (N)
Samples on Interface (SonI)	1-8	
Data interface (no mapper)	32b per lane in 8b10b 64b per lane in 64b66b	Xilinx AXI4-stream compliant
SerDes interface	10-80 bits per lane	
CPU Interface	32 bits	APB / AXI4-lite / Avalon
Deliverables		
Code	SystemVerilog	Source code or Encrypted RTL
Documentation	Yes	Including User Manual, Release Note and Quick Start Guide
Simulation Environment	Yes	System Verilog Testbench, Test Scripts
Timing Constraints in Synopsys SDC Format	Yes	
Access to Support System	Yes	
Synopsys SGDC Files	Yes	
Synopsys Lint and CDC Waivers	Yes	
Verification report	Yes	
Items available for purchase		
SystemVerilog UVM VIP	Yes	Encrypted
HW Validation Platform	Yes	AMD (Xilinx) Ultrascale demo platform available for easy testing

Size Estimates

Size estimates depend on generic settings and compile time parameter. Estimates for ASIC and FPGA are available on request and under NDA. Please contact sales@chipinterfaces.com for more information.

Ordering Info

Delivery Option code	Delivery Option
B	RTL Source Code
D	Encrypted RTL

* Encryption method supported in Cadence and Synopsis. Other can be supported on request

Technology code	Target Technology
A	ASIC
F	FPGA

Model code	Model description
IP core	
01	JESD204C RX Link layer
02	JESD204C RX Link and transport layer
03	JESD204C TX Link layer
04	JESD204C TX Link and transport layer
05	JESD204C RX + TX Link layer
06	JESD204C All
Verification Component	
CV_JESD204C_01	JESD204C UVM VIP (Encrypted SystemVerilog)