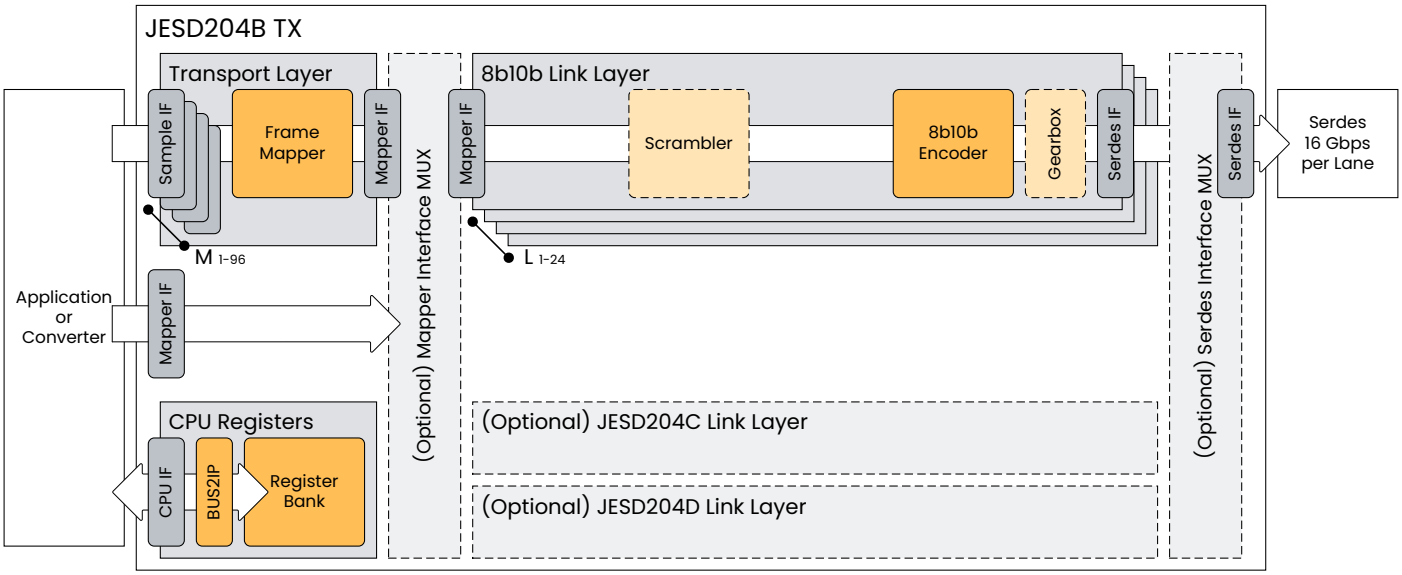
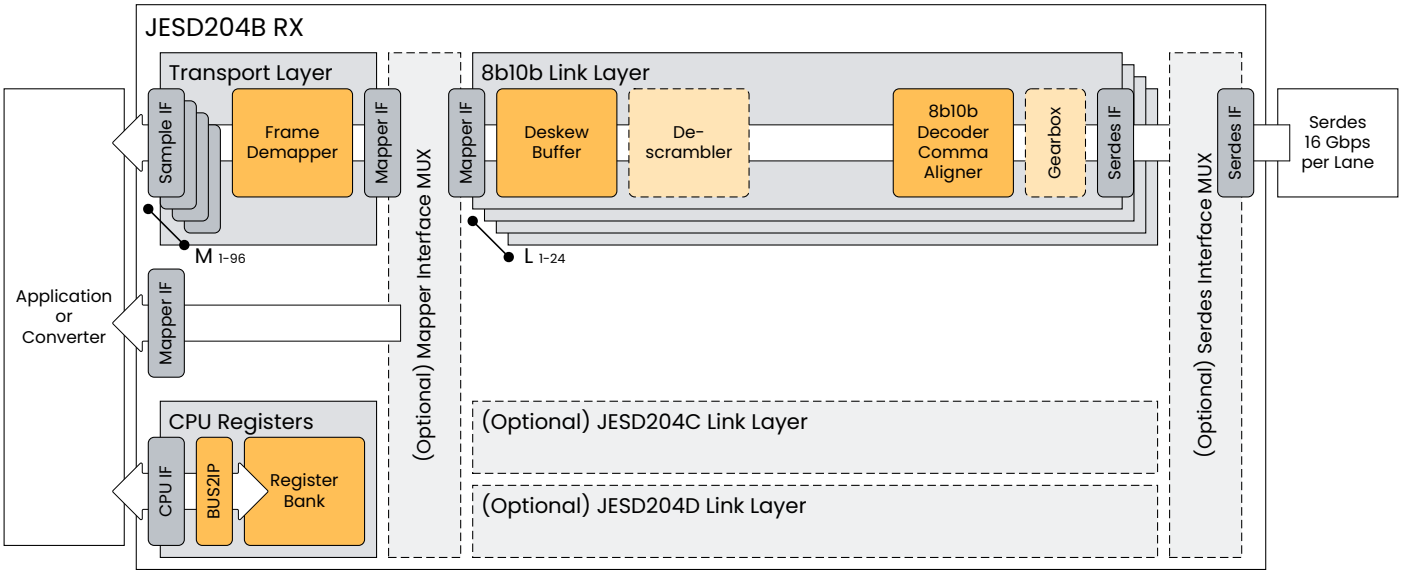
JESD204B IP Core

Datasheet V. 1.0 - July 2025

Overview

The JESD204B controller IP is a highly optimized and silicon agnostic implementation of the JEDEC JESD204B.01 serial interface standard targeting both ASICs and FPGAs. The solution by default provides line-speeds of up to 12.5 Gbps per lane while guaranteeing data alignment and synchronization. The standard allows it to optionally by used up to 16 Gbps, but does not recommend running it faster due to the 8b10b encoding. The core enables quick and reliable deployment of both the transmitter (TX) and the receiver (RX) and comes optionally with a tightly integrated transport layer option, that can dynamically be configured to handle any Multiple-Converter Device Alignment, Multiple Lanes (MCDAML) requirements. The IP comes with the widest parameter set available and has gone through extensive testing. The IP core is silicon proven, heavily tested in UVM regression environment and has been interoperability tested with key Data Converter ADC/DAC providers and leading SerDes PHY solutions.





Key Features

Richly Featured	Link and Transport layer available Scrambling and de-scrambling included Build-in test functions Support for all subclasses (0. 1. 2)
Solid	Silicon proven Lint/CDC optimized UVM regression tested with full coverage Interoperability tested with leading PHY/SerDes/ADC/DAC vendors
Easy to use	Solid documentation including integration guide Easy to use RTL test environment Strong engineering support for bring-up
Silicon Agnostic	Targeting both ASICs and FPGAs

Specification

Feature	Performance/Availability	Comment
General Features		
Standards	JEDEC JESD204B.01	January 2012
Technology	Verilog/System Verilog	For ASIC and FPGA
Line Rates	Up to 12,5 Gbps	
	Up to 16 Gbps	Optional in the Standard
	Up to 25 Gbps	Not recommended with DFE
Lanes (L)	1-24	Runtime Configurable
Number of converters (M)	1-96	Runtime Configurable
Frame Size (F)	1-255	Link layer
	1-96	Transport layer
Converter Samples per frame (S)	1-8	Runtime Configurable
Sample Widths (N)	8-32	Runtime Configurable
Total number of bits per sample in the user data format (N')	8, 12, 16, 20, 24, 28, 32	Runtime Configurable
Control bits per sample (CS)	0-3	Runtime Configurable
Control Words (CF)	0-1	Runtime Configurable
HD mode	0-1	Runtime Configurable
Mandatory Test Cases	Supported	Debug signals can be provided
Debug	Yes	
Test features	LL_8b10b - continuous K28.5, Repeated ILAS, Continous D21.5, 50 Octet JSPAT, JTSPAT, PRBS15 and Continous Low Freq Pattern	Runtime Configurable
	TL - Short Test Pattern Long Test Pattern	

Feature	Performance/Availability	Comment
8b10b		
Multi frame (K)	1-256	Runtime Configurable
Subclasses	0, 1, 2	Runtime Configurable
Receiver/Transmitter		
PCS (8b10b coding)	Yes	Can optionally be bypassed
Scrambling	Yes	Can optionally be bypassed
Interfaces		
Data interface (with mapper)	Data (MxSonIxN) Control bits (MxSonIx3)	Depends on the number of Converters (M) and Number of Samples on Interface (SonI) and bits per sample (N)
Samples on Interface (SonI)	1-8	
Data interface (no mapper)	32 bits per lane	Xilinx AXI4-stream compliant
SerDes interface (excl. PHY)	10, 20, 40 bits encoded per lane	8, 16 or 32 bits un-encoded per lane
CPU interface	32 bits	APB / AXI4-lite / Avalon
Deliverables		
Code	SystemVerilog	Source Code or Encrypted RTL
Documentation	Yes	Including User Manual, Release Note and Quick Start Guide
Simulation Environment	Yes	Simple Test Environment, Test Cases and Test Scripts
Timing Constraints in Synopsys SDC format	Yes	
Access to Support System	Yes	
Synopsys SGDC Files	Yes	
Synopsys Lint, CDC and Waivers	Yes	
Test Report	Yes	
Items available for purchase		
SystemVerilog UVM VIP	Yes	Encrypted
HW Validation Platform	Yes	Xilinx Ultrascale demo platform available for easy testing

Size Estimates

Size estimates depend on generic settings and compile time parameter. Estimates for ASIC and FPGA are available on request and under NDA. Please contact sales@chipinterfaces.com for more information.

Ordering Info

Delivery Option code	Delivery Option
B	RTL Source Code
D	Encrypted RTL

* Encryption method supported in Cadence and Synopsis. Other can be supported on request

Technology code	Target Technology
A	ASIC
F	FPGA

Model code	Model description
IP core	
01	JESD204B RX Link layer
02	JESD204B RX Link and transport layer
03	JESD204B TX Link layer
04	JESD204B TX Link and transport layer
05	JESD204B RX + TX Link layer
06	JESD204B All
Verification Component	
CV_JESD204B_01	JESD204B UVM VIP (Encrypted SystemVerilog)