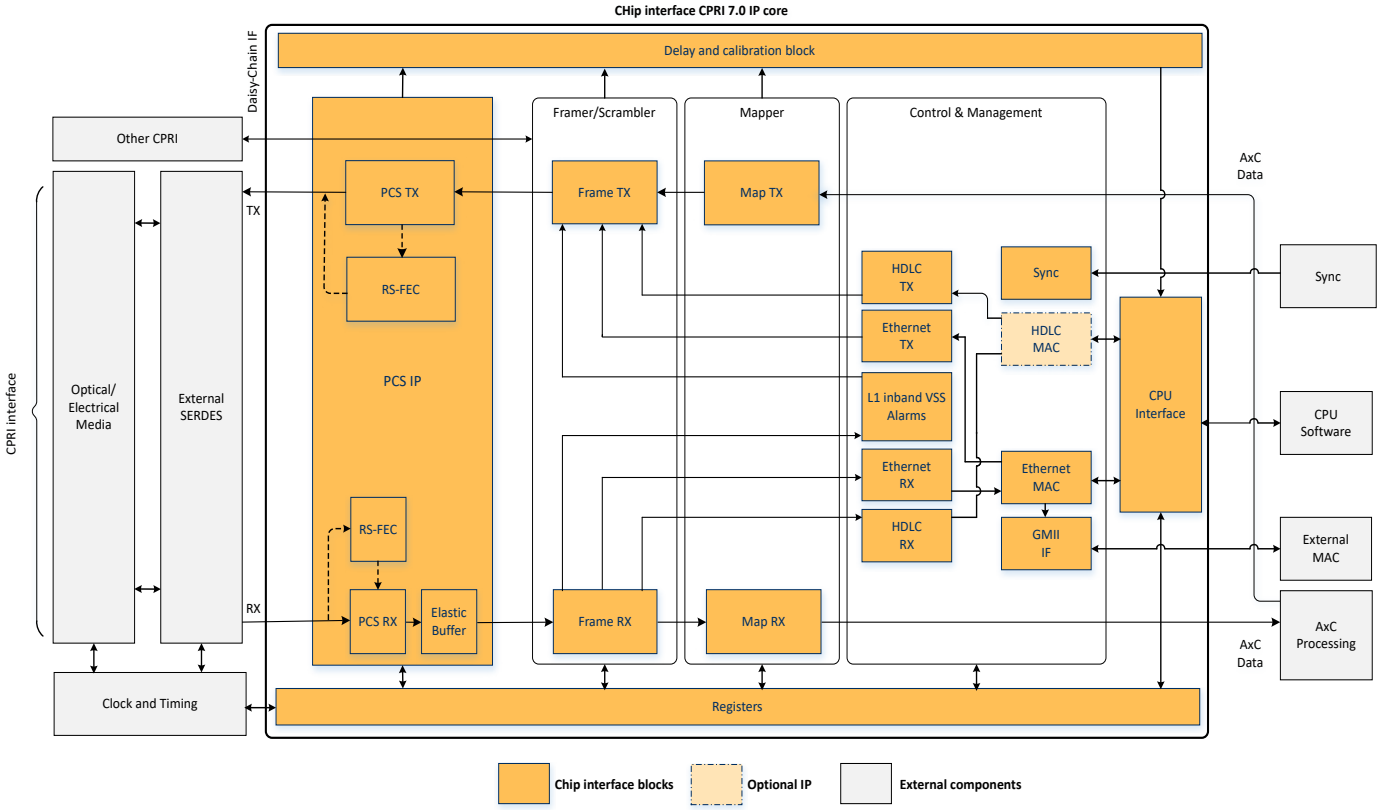
CPRI 7.0 IP Core

Datasheet V.2.5 - 23 Jan 2023

Overview

Comcores IP core is a silicon agnostic implementation of the CPRI 7.0 standard targeting both ASICs and FPGAs. With its extreme flexibility, high performance and reduced logic consumption, the CPRI IP core is the perfect match whether the application is RE (Radio Equipment) or REC (Radio Equipment Controller). It is designed to meet the requirements of Radio systems, base band systems, C-RAN switches, Digital Front-End (DFE) processors or advanced test systems. The core can be dynamically configured to handle wireless multi-mode radio systems implementing deterministic latency features and high-performance throughputs required by LTE-A and 5G radio base stations.



Key Features:

Richly Featured	CPRI Specification V7.0 full feature set All mapping methods available (method 2 and 3 are optional) Accurate delay measurements and calibration Size optimized Ethernet GMII interface
Easy to use	Testbench with typical system configuration and examples Easy integration
Highly Configurable	Modular design with full feature set available Up to 64 antenna carriers per core supported Support line-rates options 1-10 (up to 24.33024 Gbit/s) Dynamic mapping configuration
Silicon Agnostic	Designed in VHDL and targeting both ASICs and FPGA

Specification

Feature	Availability	Default	Option	Comment
General Features				
Standard	CPRI Specification V7.0	✓		
Technology	VHDL	✓		For ASIC and FPGA
Applications	RE /REC	✓		Master or slave sup-
Line Baud Rates	From 614.4 - 24330,24 Mbps	✓		All 10 line bit rate options are
Air Interfaces	W-CDMA/LTE	✓		
	WiMAX		✓	
# of Data Carriers	Up to 64 AxC	✓		Programmable
Sample Widths	8-16 bits	✓		Two options available
Mapping Methods	1	✓		
	2,3		✓	
Daisy Chaining Interface	Yes	✓		
Rate Auto-Negotiation	Yes	✓		Line-rates are program-mable
Debug	Yes		✓	Debug signals can be provided
PCS Receiver/Transmitter				
PCS (Delay Measurement, 64b66b)	Yes	✓		
Scrambling	Yes	✓		
RS-FEC	Yes	✓		PCS layer is delivered as separate IP
Control & Management				
HDLC	yes		✓	
VSS	yes	✓		CPU or AUX interface
L1-inband	yes	✓		CPU or AUX interface
Synchronization	yes	✓		CPU or AUX interface
Interfaces				
Common memory IQ Carrier	64 bits	✓		
SerDes interface (excl. PHY) 8b10b	10/20/40/80 bits encoded	✓		8, 16 or 32 bits un-encod-ed. PCS layer is delivered as separate IP
SerDes interface (excl. PHY) 64b66b	32/33/64/66 bits encoded	✓		PCS layer is delivered as separate IP
AUX interface for chaining	32 bits + frame counters	✓		
CPU interface	32 bits	✓		
AUX interface for chaining	32 bits + frame counters	✓		
Ethernet	GMII	✓		
Deliverables				
Code	VHDL	✓		Default delivered in En-crypted RTL.

Specification

Feature	Availability	Default	Option	Comment
Deliverables				
Documentation	Yes	✓		Including User Manual and Release
Simulation Environment	Yes	✓		Simple Test Environment, Test Cases
Access to Support System	Yes	✓		

Ordering Info

Delivery Option code

Delivery Option code	Delivery Option
B	RTL Source Code
C	Encrypted FPGA Netlist
D	Encrypted RTL

* Encryption method supported in Cadence and Synopsis. Other can be supported on request

Technology code	Target Technology
A	ASIC
F	FPGA

Model code	Model description
IP core	
02	CPRI 7.0 controller