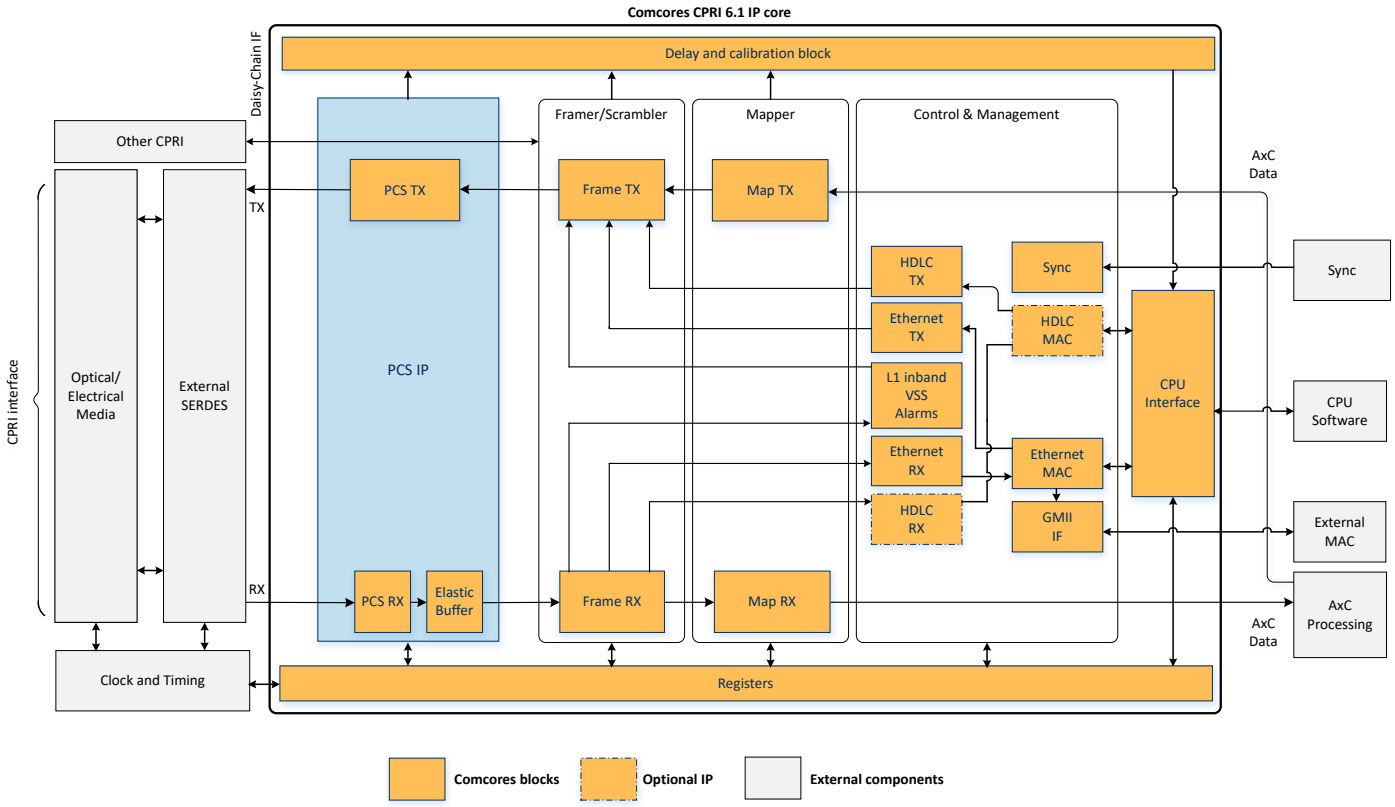
CPRI 6.1 IP Core

Datasheet V.2.6 - 23 Jan 2023

Overview

Chip Interfaces IP Core is a silicon agnostic implementation of the CPRI 6.1 standard targeting any ASIC and FPGA. With its extreme flexibility and reduced logic consumption, the CPRI 6.1 IP core is the perfect match whether the application is RE (Radio Equipment) or REC (Radio Equipment Controller). It is designed to meet or exceed the requirements of base band systems, C-RAN switches, Digital Front-End (DFE) processors or advanced test systems. The core can be dynamically configured to handle wireless multi-mode radio systems implementing deterministic latency features and high-performance throughputs required by LTE-A and 5G radio base stations



Key Features:

Richly Featured	CPRI Specification V6.1 features implemented All mapping methods available (2 and 3 are optional) Accurate delay measurements and calibration Size optimized Ethernet GMII interface
Easy to use	Testbench with typical system configuration and examples Easy integration
Highly Configurable	Modular design with full feature set available Up to 64 antenna carriers per core Support line-rates 1-9 (up to 12165.12 Mbit/s) Dynamic mapping configuration
Silicon Agnostic	Designed in VHDL and targeting both ASICs and FPGAs

Specification

Feature	Availability	Default	Option	Comment
General Features				
Standard	CPRI Specification V6.1	✓		
Technology	VHDL	✓		
Applications	RE /REC	✓		Master or slave supported
Line Baud Rates	From 614.4 - 12165.12 Mbps	✓		All 9 line bit rate options
Air Interfaces	W-CDMA/LTE/WiMAX	✓		3GPP UTRA /E-UTRA/GSM-EDGE,
# of Data Carriers	# of Data Carriers	✓		Programmable
Sample Widths	8-20 bits	✓		Two options available
Mapping Methods	1, 3	✓		
	2		✓	
Daisy Chaining Interface	Yes	✓		
Rate Auto-Negotiation	Yes	✓		Line-rates are program-mable
Debug	Yes		✓	Debug signals can be pro-vided
Receiver/Transmitter				
PCS (Delay Measurement, 64b66b)	Yes		✓	Can be purchased as a separate item
Scrambling	Yes	✓		
RS-FEC	Yes		✓	Can be purchased as a separate item
Control & Management				
Ethernet	yes	✓		
HDLC	yes		✓	
VSS	yes	✓		CPU or AUX interface
L1-inband	yes	✓		CPU or AUX interface
Synchronization	yes	✓		CPU or AUX interface
Interfaces				
Common memory IQ Carrier	32 bits	✓		
SerDes interface (excl. PHY)	10,20 or 40 bits encoded	✓		8, 16 or 32 bits unencoded
CPU interface	32 bits	✓		
AUX interface for chaining	32 bits + frame counters	✓		
GMII	yes	✓		
HDLC interface	yes		✓	
Deliverables				
Code	VHDL	✓		
Documentation	yes	✓		Including User Manual and

Specification

Feature	Availability	Default	Option	Comment
Deliverables				
Simulation Environment	Yes	✓		Simple Test Environment, Test Cases
Timing Constraints in Synopsys SDC	Yes	✓		
Access to Support System	Yes	✓		
Synopsys Lint and CDC	Yes		✓	

Ordering Info

Delivery Option code

Delivery Option code	Delivery Option
B	RTL Source Code
C	Encrypted FPGA Netlist
D	Encrypted RTL

* Encryption method supported in Cadence and Synopsis. Other can be supported on request

Technology code	Target Technology
A	ASIC
F	FPGA

Model code	Model description
IP core	
01	CPRI 6.1 controller