CS6100

Product Brief JPEG Encoder

The CS6100 Motion JPEG (M-JPEG) Encoder is a highly integrated virtual component solution for leading-edge image compression and transmission applications. It is capable of sustaining a throughput of 1 sample per clock cycle – with the clock rate being silicon process dependent. Equally suited to low-power, battery-operated consumer electronics as it is to high-end professional video equipment and office automation solutions, the CS6100 delivers the optimal performance and low power consumption that only an application specific virtual component (ASVC) can provide. The CS6100 is available in both SoC and programmable logic versions that have been designed by Amphion to deliver high performance with low-power and minimal silicon area.

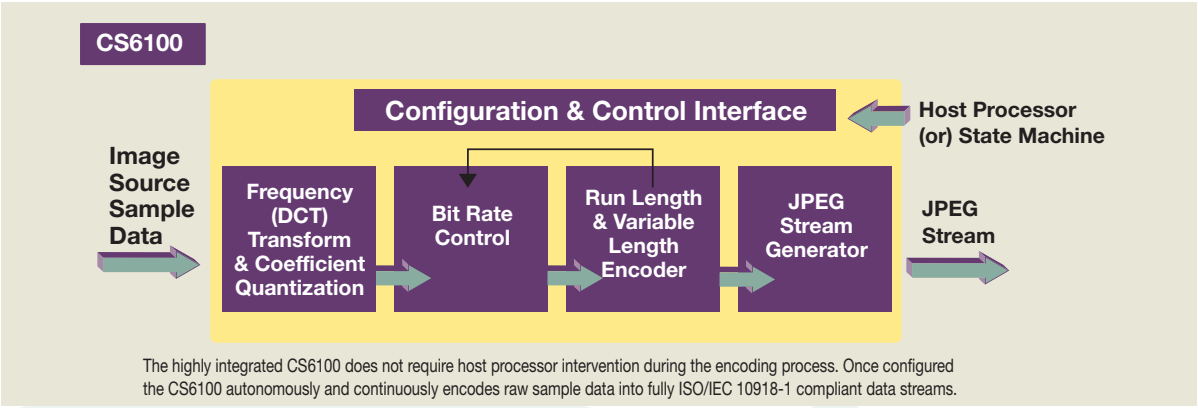

Figure 1: CS6100 Overview Diagram

FEATURES

- **High Performance**
  - Single sample per clock cycle processing
- **Low Power**
  - Fully synchronous operation
  - Zero-power standby mode[3]
- **Fully Compliant with Baseline JPEG Standard ISO/IEC 10918-1/2**
- **Autonomous Operation**
  - Sample data in, JPEG stream out
  - No host processor intervention required
- **Dual Mode Operation**
  - AutoMode™ continuous streaming mode
  - Variable image mode
- **Ease of Integration**
  - Tapeout-Ready™ Firm-IP targeted netlist
  - No code memory required
  - TestReady™ netlist configuration
- **Advanced Image Coding Features**
  - Four programmable quantization tables
  - Four programmable Huffman Coding Tables
  - Bit-rate control for dynamic output rate stabilization (patent pending)
  - On-board configuration data memory
- **Ease of Configuration**
  - State machine: synchronous handshake interface
  - Host Processor: memory mapped interface capability
  - Support for standard and abbreviated JPEG configuration formats
  - AutoMode™ configure-once encode-many operation
- **Flexible Image Source Input**
  - Image Size up to 65,535 by 65,535 (4.3 Gigapixel)
  - All color formats including: RGB, YUV, YCbCr, CMYK and Grayscale
  - Horizontal and vertical sub-sampled input supported
  - Interleaved and non-interleaved scans supported

KEY METRICS

- **Logic:** 72K gates (std cell)
- **Memory:** 21.6K bits RAM (5 blocks)

APPLICATIONS

- **Digital Still Cameras:**
- **Remote Digital Video:**
- **Video Production:**
- **Office Automation Equipment:**
- **Handheld Scanners:**

1) Performance is dependent on the silicon process and libraries selected.
2) 30 frame/sec, 24-bit color images with three components in 4:2:0 format.
3) When implemented with fully static SRAM blocks w/power-down.

CS6100 FUNCTIONAL DESCRIPTION

The CS6100 ASVC is a highly integrated JPEG encoder suitable for a wide range of imaging applications. Designed for continuous data flow – one image sample per clock cycle – without host microprocessor intervention, the CS6100 can address the most demanding frame-based video compression applications. In addition, it is ideal for low power applications where – once configured – it can be stopped and restarted instantaneously. The fully synchronous, highly autonomous design requires no software overhead. A rich feature set includes an adaptive-feedback bit rate control (BRC) mechanism (patent pending), multiple real-time selectable coding tables, manual and automatic configuration modes and on-board configuration memory. The CS6100 is a powerful and flexible JPEG encoding solution.

FUNCTIONAL BLOCK OVERVIEW

Image source data in any color space format is input to the CS6100 in block data format. The CS6100 can process up to 255 color components in an unlimited number of scans per image (each scan can contain between one and four color components). The image samples are compressed accordingto user-definable quantization and Huffman coding parameters. Built-in bit rate control circuitry is selectively employed for bandwidth constrained applications. The CS6100 outputs an ISO/IEC 10918-1 compliant data stream. Separate configuration, parameter extraction and test access ports provide high visibility and flexible control for ease of integration of the CS6100 into the complete system-level SoC design.

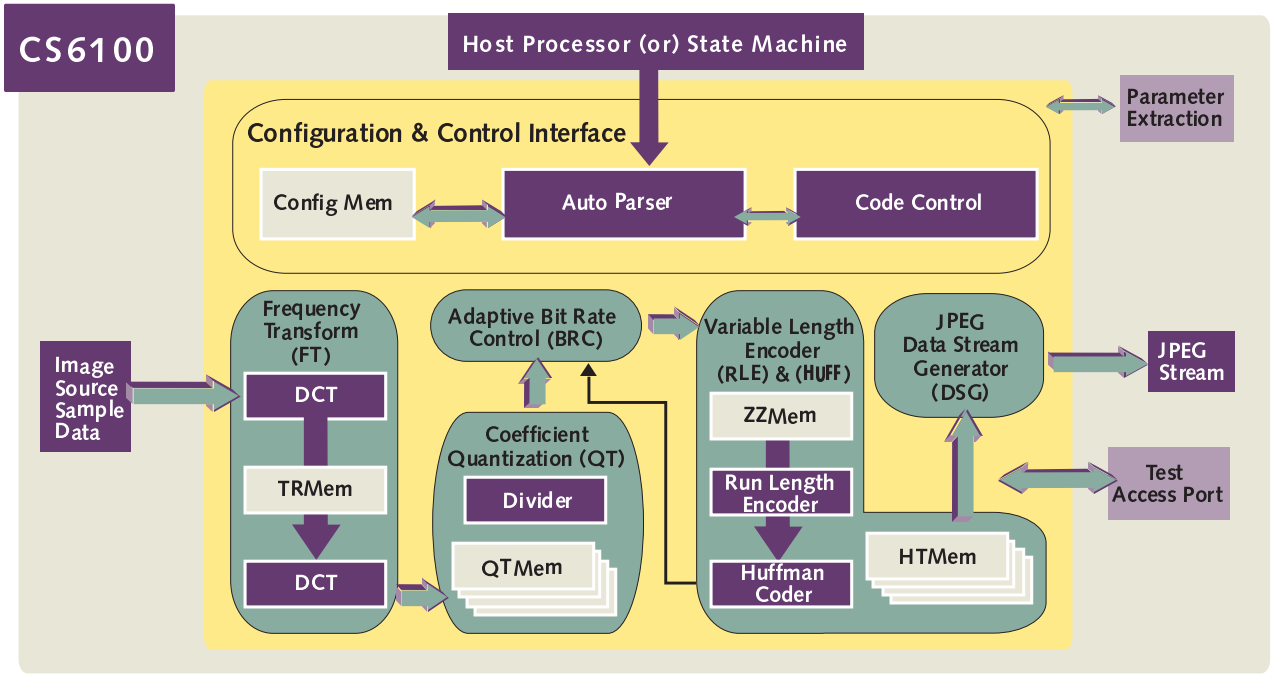

Figure 2: CS6100 JPEG Encoder block diagram

AVAILABILITY AND IMPLEMENTATION INFORMATION

DELIVERABLES

- Targeted optimized netlist for chosen technology (SoC or FPGA)
- Bit-accurate C-model
- Simulation model for system integration
- Technical support
- Test Suite (standalone self-checking test-bench which incorporates control software via PLI with reference test data)
- Synthesis scripts
- Documentation (Integration, Simulation, Application and Function databooks)

ABOUT AMPHION

Amphion is the leading supplier of silicon-proven semiconductor intellectual-property (IP) for digital video and imaging System-on-a-Chip (SoC), ASIC and programmable logic (FPGA) designs, delivering high performance solutions for video and image compression with a comprehensive range of silicon-optimized products. Amphion develops and licenses semiconductor IP cores that are close to optimal in terms of power, cycles, and area. Amphion cores operate standalone, or by in conjunction with industry-standard RISC processors, and can be easily migrated through successive generations of fabrication technology.

HEADQUARTERS

Amphion Semiconductor Ltd
Suite 7, Linden House
Beechill Business Park
Beechill Road
Belfast BT8 7QN
Northern Ireland, UK

Tel: +44 28 95 609 600

Web: www.amphionsemi.com
Email: info@amphionsemi.com

SALES AGENTS

SPINNAKER SYSTEMS INC.
Shin-Yokahama
Fujika Bldg. 8F
2-5-9 Shin Yokahama
Kouhoku-Ku
Yokohama 222-0033 Japan
Tel: +81.3.3551.2275
Fax: +81.3.3551.2614
Email: info@spinnaker.co.jp
http://www.spinnaker.co.jp/