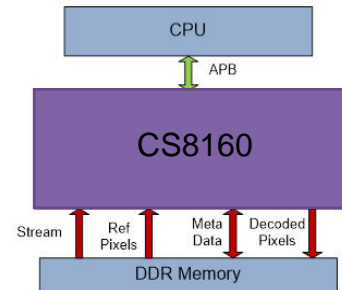


Production Proven – HEVC/H.265 8Kp60 – Video Decoder

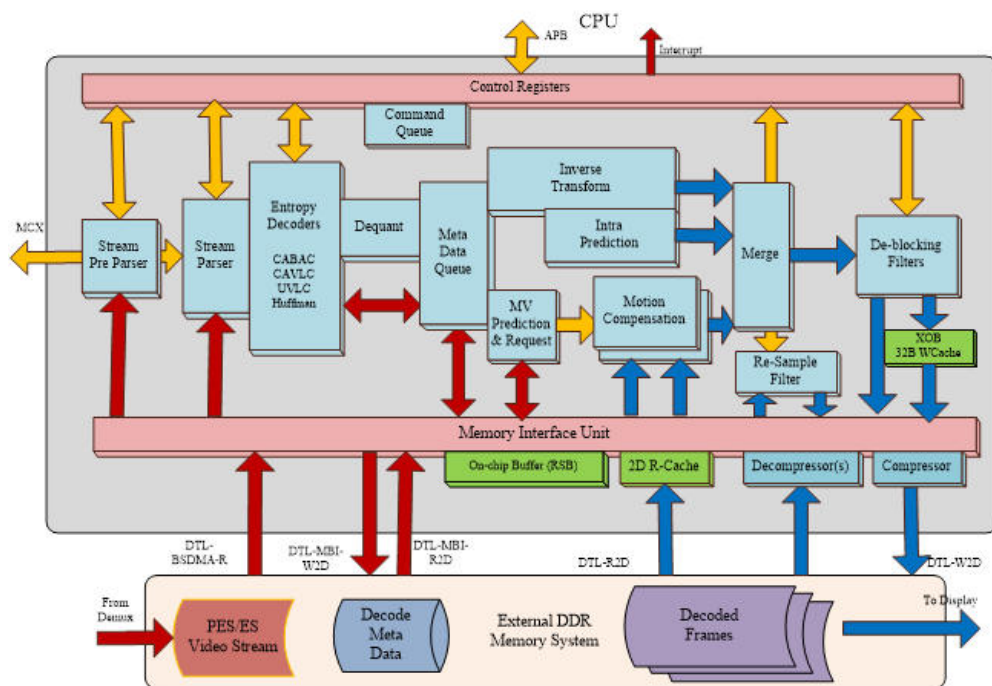
- High resolution video decoder
- Technology silicon proven in multiple STB and DTV chipsets
- Hardware decoder paired with a RISC controller to perform video decode

Features
<ul style="list-style-type: none"> • HEVC/H.265 MP@L6.1 (8KP60) • PES or ES stream input • High Latency Tolerance (CPU & Memory) • Low CPU load • Low Memory Bandwidth • Robust Error Resilience controlled by Firmware • Mature technology silicon proven in multiple mass production STB and DTV SoCs down to 28nm • Production Verified Firmware • Extensively verified with a large library of third party test streams.



Operation

- CS8160 operates under direction of firmware
- Firmware pre-decodes headers and banks configuration commands
- Low CPU load allows CPU to run other hardware blocks in the system



CS8160 Block Diagram

Deliverables

- Bit accurate C models
- Verilog RTL and production firmware
- Synthesis scripts
- Self-checking test environment
- Datasheet and user manual

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