CS6650

Product Brief HD MPEG-2 Video Decoder

The CS6650 high-definition MPEG2 decoder is designed to provide high performance solutions for a broad range of motion image applications. This highly integrated application specific core is developed for standard definition video, compliant with ISO/IEC 13818-2 (MPEG2) and capable of decoding video streams up to 4:2:2 Profile at High Level (422@HL). The CS6650 is equally at home in mainstream consumer applications, decoding 4:2:0 bitstreams at High or Main Level (MP@HL) and can also decode MPEG1 (ISO/IEC 11172-2) bitstreams. The CS6650 is available for both SoC and the main FPGA technologies and has been optimized for performance while minimizing area.

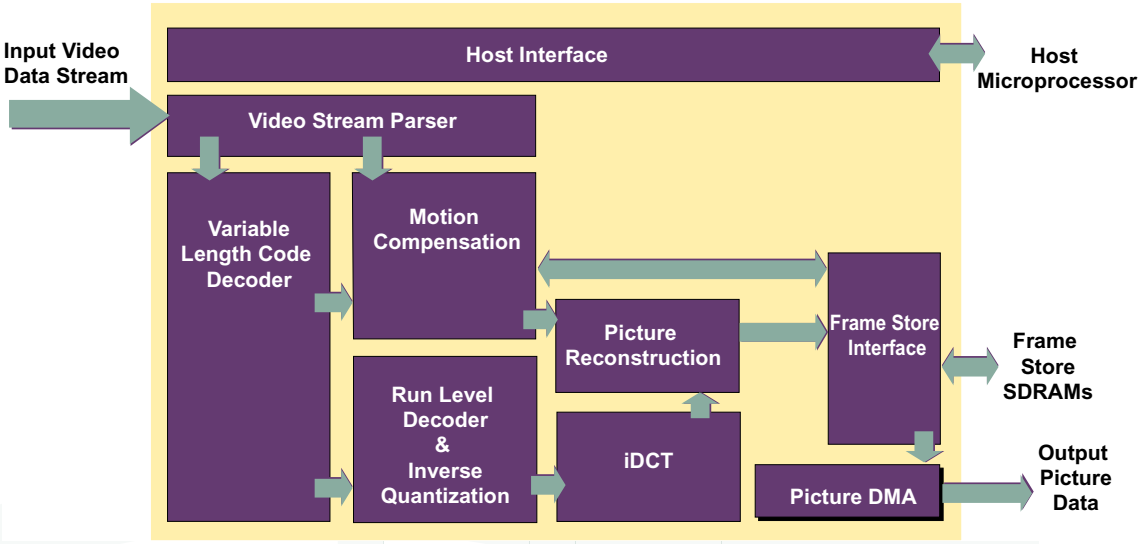

Figure 1: CS6650 Overview Diagram

DECODER FEATURES

- **Supports progressive scan and interlaced streams**
- **ISO/IEC 13818-2 (H.262) Compliant**
  - MP@ML through 4:2:2@HL
  - Decodes ISO/IEC11172-2 (MPEG1) Constrained Parameter bitstreams
- **High performance solution for high data rate MPEG2 decoding**
  - Supports input bit rates up to 300Mbit/sec
  - Real time decode and display of 4:2:2@HL
- **Supports all ATSC and HDTV defined resolutions and frame rates**
- **Bitstream error detection and recovery**
- **Glueless interface to external DRAM**
- **Capable of standalone stream decoding or host CPU controlled operation**
- **Fully synchronous design with host shutdown and restart control**
- **Ease of integration**

KEY METRICS AND SPECIFICATION

- **Logic:** 105k gates
- **Memory:**
  - 1.5Kbytes (internal)
  - 128 MBit (external)
- **Input clock:** 133 MHz (min)

APPLICATIONS

- **Digital cable and satellite set-top decoder box for ATSC and HDTV**
- **DVD - standard and high definition**
- **PC video hardware accelerator**
- **Studio 4:2:2 editing or production**

CS6650 FUNCTIONAL DESCRIPTION

The CS6650 core is a highly integrated MPEG2 video decoder suitable for a wide range of video applications. The CS6650 accepts the input video elementary stream as aligned bytes from conditional access decryption, transport stream demulti-plexer, or similar source. The core can operate in a default mode on an input stream without the intervention of a host CPU. In this mode pictures will be decoded from the video stream and output in correctdisplay order. A host CPU has access to a full range of information and control to manipulate the behavior of the decoder topermit audio/video synchronization, pan and scan and letterbox conversion, and various trick modes. The output from the core is provided by a highly configurable pixel stream DMA (Direct Memory Access) engine. This engineallows adjustable output video component sequencing and provides external logic with control over the display of the picture.

FUNCTIONAL BLOCK OVERVIEW

VIDEO STREAM PARSER

The Video Stream Parser unit extracts various encoding parameters from the input video stream and any requested user specific data contained within the stream, such as closed-caption or teletext data. This information is contained in headers at each layer of the stream and may be used throughout the rest of the decoding and reconstruction process. Selected user data is stored to buffer space and made available to the host CPU. Having removed header information from the stream, the Video Stream Parser unit passes the variable length encoded picture data to the Variable Length Code (VLC) Decoder unit. A range of parameters describing the overall stream and the picture currently being decoded is made available to the rest of the decoder.

VARIABLE LENGTH CODE DECODER

The Variable Length Code Decoder unit decodes the Huffman-style variable length encoded picture data. The outputs of this unit include the Discrete Cosine Transform (DCT) block run-level information for the Inverse DCT (iDCT) unit and decoded macroblock motion vectors for the motion compensation unit as well as a number of information fields describing the section of the picture currently being decoded. These decoded fields are made available to the rest of the decoder.

RUN-LEVEL DECODER & INVERSE QUANTIZATION

The output run-level information from the VLC decoder is converted into complete blocks of 64 quantized DCT coefficients by the Run-Level decoder. These coefficients are passed to the Inverse Quantizer for conversion back to actual DCT coefficients. To perform this, the Inverse Quantizer keeps track of a number of tables and scale factors, all extracted from the input video stream.

INVERSE DCT

This high performance unit performs the inverse quantization of 8x8 DCT-encoded Y, Cr and Cb pixel blocks. This key unit is capable of streaming data through continuously, transforming, every 64 clock cycles, an entire block of 8x8 DCT coefficients into an 8x8 block of pixel samples or estimated sample corrections.

MOTION COMPENSATION

Where the video data is encoded as an estimate using previous pictures and a set of corrections, the Motion Compensation unit forms the estimated pixel values. The Motion Compensation unit takes decoded motion vectors from the Variable Length Code Decoder unit and translates them into row and column coordinates within the pictures from which the estimations are being made. The reference samples for these coordinates are requested from the Frame Store Interface and the resulting pixels combined where necessary to form the estimated values for the block being decoded.

PICTURE RECONSTRUCTION

The Picture Reconstruction unit combines decoded pixels or corrections from the iDCT unit with the estimated pixels from the Motion Compensation Unit and writes the resulting pixels to the Frame Store, ready for subsequent display or reference.

FRAME STORE INTERFACE

The Frame Store is required for the storage of the two reference pictures used in the MPEG2 algorithm to form the estimated pixels. It also stores the frame currently being decoded and another frame currently being displayed. This allows the decoding and the display operations to be decoupled making audio/video synchronization simpler to maintain.

The Frame Store is implemented using two SDRAM chips which are commodity PC133 64Mbit parts, each with 2Mx32 organization. The memory interface runs at 133MHz and can be directly connected to the SDRAM chips using suitable pads.

The Frame Store SDRAM Interface handles the mapping of pixel read and write requests from the Motion Compensation, Picture Reconstruction and Picture DMA units into linear memory addresses. Additionally, the host interface can access the memory banks. Arbitration between the various accessing units and memory transaction queues are all maintained by the SDRAM Interface.

PICTURE DISPLAY DMA

The Picture Display DMA has a double-byte output interface which can carry Y, Cr or Cb pixel data. Y and Cr or Cb data can be output simultaneously as 16-bit wide values or sequentially as four separate bytes. For 4:2:0 video streams the Picture Display DMA unit will upsample the chrominance vertically to provide a 4:2:2 output. The Display DMA engine has the capability to be programmed by the host CPU to display only a certain portion of the picture or, in stand-alone mode, will display the entire coded picture.

A number of handshake signals are provided on the Picture Display DMA interface to allow the external logic to control the timing of the pixel output stream and to control the end of the current scan row or picture display. Outputs indicate to the external logic the nature of the pixel being currently driven; the end of row and end of picture flags are available to allow, for example, sync pulse generation.

HOST INTERFACE

When the CS6650 is operating with the assistance of a host CPU, a number of additional features can be accessed. All interfacing between the host and the CS6650 is performed through the Host Interface unit. This unit allows read/write access to all the internal control, status and video stream parameter registers contained within the decoder.

The Host Interface also provides a simple 32-bit read/write access to the Frame Store SDRAM. Normally, the areas of the SDRAM used for storage of picture data cannot be accessed by the Host Interface; however, a bypass mode allowing direct access is provided for system diagnostic tests, etc.

A number of conditions arising from the decoding of the video stream may require the software on the CPU to be alerted. An interrupt controller within the Host Interface unit provides a simple Interrupt Request signal and an interrupt status and mask register.

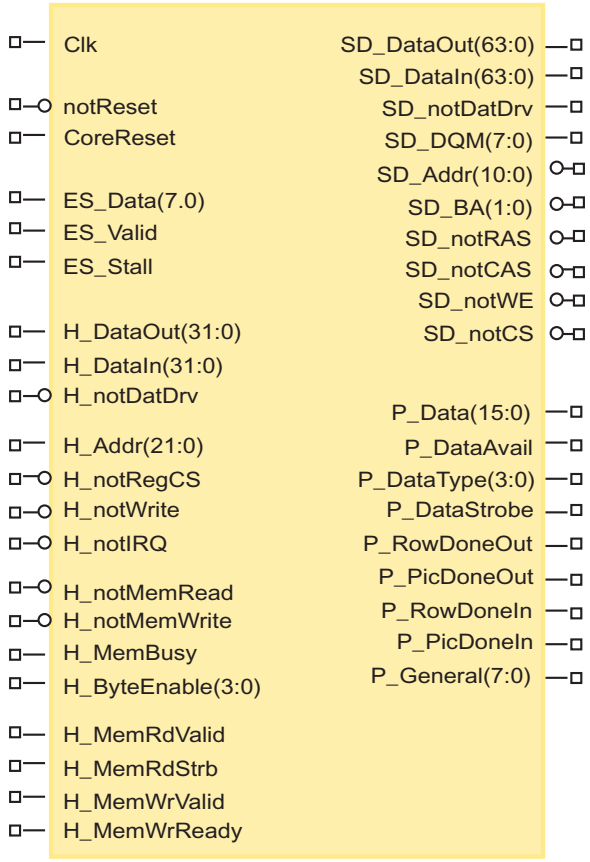

Figure 2: CS6650 Symbol and Pin Description

MEMORY BLOCK	CONFIGURATION (WORDS X BITS)	PORTS
iDCT Transpose Memory	64 x 16	Dual Port, synchronous
Quantizer Matrix Memory	256 x 8	Single Port, synchronous
Scan Conversion Memory	64 x 12 (x2)	Single Port, synchronous
Macroblock Store	32 x 64 32 x 72 16 x 64	Dual Port, synchronous Dual Port, synchronous Single Port, synchronous
Display DMA engine	32 x 64	Dual Port, synchronous
User Data Store	256 x 8	Single Port, synchronous

DELIVERABLES

- Targeted optimized netlist for chosen technology (SoC or FPGA)
- Bit-accurate C-model
- Simulation model for system integration
- Technical support
- Test Suite (standalone self-checking test-bench which incorporates control software via PLI with reference test data)
- Synthesis scripts
- Documentation (Integration, Simulation, Application and Function databooks)

ABOUT AMPHION

Amphion is the leading supplier of silicon-proven semiconductor intellectual-property (IP) for digital video and imaging System-on-a-Chip (SoC), ASIC and programmable logic (FPGA) designs, delivering high performance solutions for video and image compression with a comprehensive range of silicon-optimized products. Amphion develops and licenses semiconductor IP cores that are close to optimal in terms of power, cycles, and area. Amphion cores operate standalone, or by in conjunction with industry-standard RISC processors, and can be easily migrated through successive generations of fabrication technology.

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