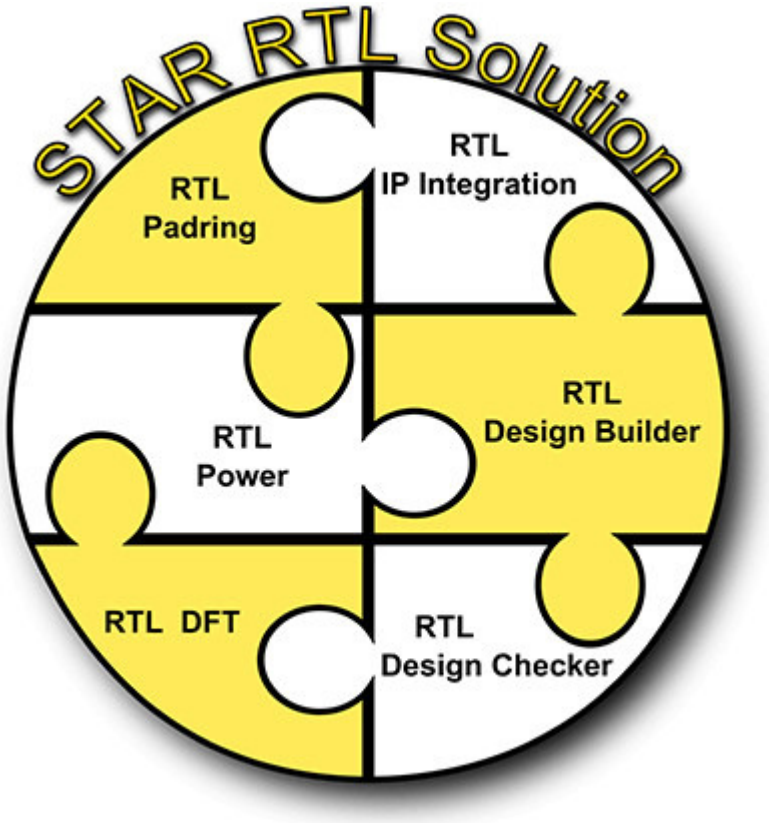
What the STAR RTL design solution is about?

STAR helps RTL designers and SoC integration teams build and generate synthesis-ready RTL code.

STAR targets RTL Structural Architectures and provides key capabilities such as building RTL code from scratch or, given existing RTL blocks/IPs. It generates new RTL for different applications such as low power design, RTL padring, DFT and many other types of applications. Also, STAR offers easy extraction of design information jointly with structural verification capabilities, simulation-free.



Through its unique “Build&Signoff” design capabilities, STAR combines in one powerful script the ability to extract design information, edit and generate the synthesizable RTL code and signoff the final RTL code. This helps run ‘what-if’ scenarios and evaluate possibilities by safely editing and generating new RTL code.

It is noteworthy that STAR extends beyond RTL! STAR supports gate-level netlists and offers multiple APIs written in a variety of languages : TCL, Perl and Java. Coherency between the RTL and different standards is a key part of the STAR design solution: typical examples are power intent for low power applications, IPXACT for IP integration, CTL for testing languages, etc.

Please refer below to the list of STAR RTL EDA tools.

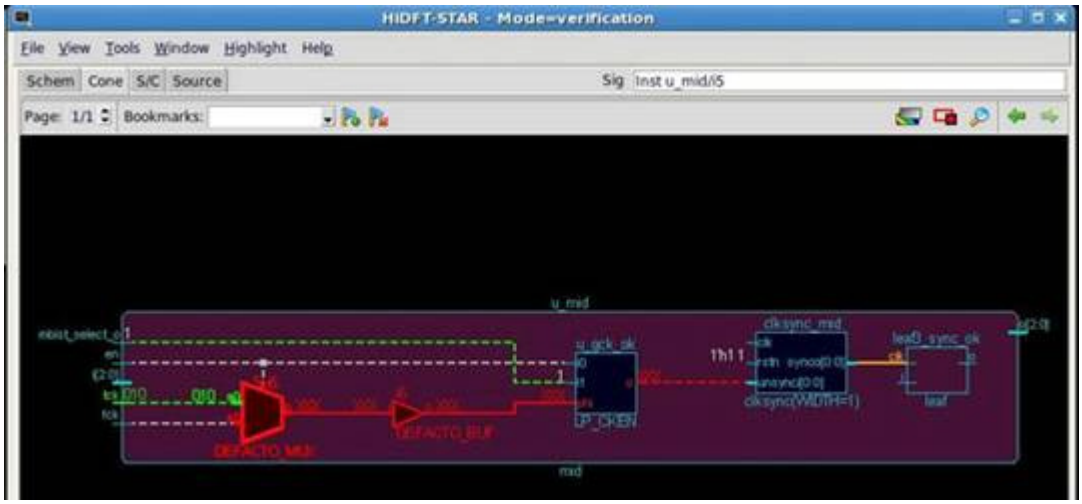
DEFACTO CREATED ITS US BRANCH.

Defacto Incorporated was created in August 2013 with an administration office in Boston area.
Both the Defacto business and technical teams are located in three areas: San Jose, San Diego and Austin.

VISIT US AT DVCON SAN JOSE.

Defacto will be exhibiting at DVcon starting March 3, 2014 at the Doubletree Hotel in San Jose. We will demonstrate the unique STAR–based RTL “Build&Signoff” design and verification methodology and also share the experience of major IDMs who are benefiting from the STAR design solution.

Highlighting RTL Design Checker



The tool automatically and cost-effectively performs general purpose connectivity checks for a large number of pins simulation-free. Typical features are:

- In-depth design exploration through a Tcl interface: Query design objects, extract fanin / fanout cone, extract hierarchical paths, signal tracing, etc.
- Simulation-free pin-to-pin tracing under different constraints

Extracted from www.deepchip.com

We use STAR extensively to check structural connections on clocks and for I/O muxing logic without doing lengthy simulations. The main purpose is to guarantee that 2 nodes are structurally connected after applying a set of constraints.

Examples:

1. The output of a specific block is directly connected to a specific chip I/O in a particular pin muxing mode.
2. A specific clock propagates from a PLL to the input of a particular clock in a defined mode, like DFT.

These pin-to-pin tracing checks (under constraints) have saved us a lot of time and effort -- especially with its GUI that can pinpoint the exact location of the blockage, if any. We use Defacto checks as a regression to make sure our subsequent RTL meets our connectivity intent.

STAR RTL EDA Tools

- **RTL Design Checker:** RTL Design exploration and simulation-free structural verification
- **RTL Design Builder:** Design Building, RTL editing with code generation of synthesizable RTL
- **RTL Design For Test** : Testability evaluation, debug and enhancement at RTL
- **RTL Padring :** Full PADring placement with RTL code generation
- **RTL Power :** Power intent exploration with design compliance
- **RTL IP Integration**: Easy IP packaging, integration and reuse
- **RTL Application Development Environment** : Build custom and language independent design environment for RTL application development

Defacto Technologies

Phone: +33-4 76 66 83 30 - www.defactotech.com - E-Mail: inforeq@defactotech.com