Arasan Chip Systems Announces the Industry First SD 4.1 Total IP Solution

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Supporting the New ADMA 3 to Maximize the Effective Throughput by Reducing the Burden on Software Driver

San Jose, California – April 18, 2013 - Arasan Chip Systems, Inc. ("Arasan"), a leading provider of Total IP Solutions for mobile applications, announced today the availability of the industry's first SD 4.1 Total IP Solution for engineering and product development of SD 4.1 devices with the UHS-II physical layer interface. Arasan is an active contributor to SDA specification. Based on its in depth involvement and knowledge of the new specification, and its field proven SD 4.0 IP, Arasan is making this new SD 4.1 total IP solution available to customers who are the leaders, providing the most advanced feature set in the mobile applications.

To meet the ever increasing data transfer rate in high end applications, such as professional broadcasting transmission or advanced high resolution display, the SD 4.1 specification calls out the maximum performance of 1.56 Gbps at UHS-II full duplex mode per lane or half duplex UHS-II at 3.16 Gbps. In real applications, due to the system overhead and different SD 4.1 device controller designs, the actual measured performance can vary dramatically from system to system. With the newly introduced ADMA 3, the OS driver is now able to issue multiple read or multiple write commands at once, without having to wait for the SD controller to complete one command at a time. Once the SD host controller has collected multiple commands, it will then manage and complete them without intervention from the host software drive. Thus, the UHS-II 1.56 Gbps interface can be more effectively utilized and maximize the system throughput. This feature can be very useful when running multithreaded applications where multiple applications are constantly updating their status or swapping their contents by writing or reading small chunk of data to or from the memory card.

Helping engineers to accelerate time to market, Arasan provides a complete suite of tools for IP integration including SD 4.1 link layer controller IP, UHS-II PHY in advanced process technologies, verification IP with robust test suite, FGPA validation and development platform, and software stack in source code. The link layer controller IP is designed with the most interoperability in place, based on Arasan's extensive experience in working with many SD host and SD device companies. Arasan has conducted several interoperability tests to ensure wide range of compatibility with different products in the market. Developed in advanced, 40nm and below process nodes, the UHS-II PHY is designed for higher signal integrity and lower power consumption compared to competition. Arasan has optimized it Linux based SD software driver and tested its performance by running the Linux storage device benchmark; the benchmark results demonstrated the software driver achieving more than 90% bandwidth efficiency to squeeze out every bit of performance improvement.

Incorporating Arasan's SD 4.1 IP on a FPGA board with the software stack on a Linux based system, Arasan provides a Hardware Validation Platform (HVP) which enables early validation of SD 4.1 specification by emulating

the SD 4.1 Host at the interface protocol level. Beyond this, it facilitates early application development for reference board designs and production testing, before the SD 4.1 memory cards are available in silicon. Further in the product cycle, the HVP acts as a reference platform to help identify any incompatibilities between the device under development, and the silicon device it is communicating with.

Availability

Arasan is engaging with customers now on the SD 4.1 Total IP Solution, including SD 4.1 Controller IP, UHS-II, Verification IP (VIP), Linux Software Stack in source code, Hardware Validation Platform (HVP), and all supporting documents.

About Arasan

Arasan Chip Systems is a leading provider of Total IP Solutions for mobile storage and connectivity applications. Arasan's high-quality, silicon-proven, Total IP Solutions include digital IP cores, analog PHY interfaces, verification IP, hardware verification kits, protocol analyzers, software stacks and drivers, and optional customization services for MIPI, USB, UFS, SD, SDIO, MMC/eMMC, UFS, and many other popular standards. Arasan's Total IP products serve system architects and chip design teams in mobile, gaming and desktop computing systems that require silicon-proven, validated IP, delivered with the ability to integrate and verify both digital, analog and software components in the shortest possible time with the lowest risk.

Unlike many other IP providers, Arasan's Total IP Solution encompasses all aspects of IP development and integration, including analog and digital cores, hardware development kits, protocol analyzers, validation IP and software stacks and drivers and optional architecture consulting and customization services. Based in San Jose, CA, USA, Arasan Chip Systems has a 17 year track record of IP and IP standards development leadership.

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