

Arasan Chip Systems Announces Industry First M-PHY 3.0 Total IP Solution

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Arasan Leads Industry with M-PHY-based Analog Interfaces for Low Power Mobile Storage

San Jose, California – October 7, 2013 - Arasan Chip Systems, Inc. ("Arasan"), a leading provider of Total IP Solutions for mobile applications, today announced the availability of the industry's first MIPI® M-PHY® 3.0-compliant IP supporting multiple speed gears and a broad range of high-speed interfaces for mobile applications. **Arasan's MIPI M-PHY version 3.0 multi-gear analog IP PHY** supports a wide selection of protocols including Universal Flash Storage (UFS), Camera Serial Interface 3 (CSI-3), USB Super-speed Inter-chip (SSIC) and M-PCIe interfaces.

"We have been licensing the Arasan M-PHY analog IP for customers' mobile application processor and memory applications for more than 18 months," stated Andrew Haines, VP of Marketing. "Leveraging our leadership position in deploying M-PHY analog IP to multiple tier-1 SoC and memory manufacturers, we have assembled a Total IP Solution for UFS consisting of UFS 2.0, UniProSM 1.6, M-PHY 3.0, UFS stack and drivers and a hardware validation platform."

Arasan Chip Systems is a contributing member of the MIPI Alliance and actively participates in the PHY Working Group. The Arasan M-PHY IP offers support for high-speed GEAR1, GEAR2 and GEAR3 supporting a wide variety of different protocol and performance requirements up to 5.8Gbps per lane. In addition, the MIPI M-PHY IP is compliant to **MIPI Alliance** Standard for M-PHY specification version 3.0, supports M-PHY Type I systems, high-speed differential and low-speed PWM modes, configurable termination, error detection and on-chip clock generation. The highly configurable M-PHY analog IP core enables designers with a scalable solution to easily meet increasing high performance data rates, modular architectures for IP re-use and customer proven silicon IP. Arasan's MIPI M-PHY analog IP implementation is optimized to support high-performance while meeting the low power, small area and optimized electromagnetic interference (EMI) performance requirements of mobile applications.

In addition, Arasan ships a **UFS Hardware Validation Platform (HVP)** enabling early validation by emulating a Host or Device system at the interface protocol level.

Availability

Arasan's M-PHY analog Total IP solution is available now, including host and device digital controllers (UFS 2.0, CSI-3), Verification IP, Linux OS-based Hardware Platforms and all of the customer-required support files and documentation.

About Arasan

Arasan Chip Systems is a leading provider of Total IP Solutions for mobile storage and connectivity applications. Arasan's high-quality, silicon-proven, Total IP Solutions include digital IP cores, analog PHY interfaces, verification IP, hardware verification kits, protocol analyzers, software stacks and drivers and optional customization services for MIPI, USB, UFS, SD, SDIO, MMC/eMMC, UFS, PCIe and many other popular standards. Arasan's Total IP products serve system architects and chip design teams in mobile, embedded and desktop computing systems that require silicon-proven, validated IP, delivered with the ability to integrate and verify both digital, analog and software components in the shortest possible time with the lowest risk.

Unlike many other IP providers, Arasan's Total IP Solution encompasses all aspects of IP development and integration, including analog and digital cores, hardware development kits, protocol analyzers, validation IP and software stacks and drivers and optional architecture consulting and customization services. Based in San Jose, CA, USA, Arasan Chip Systems has an 18 year track record of IP standards development leadership.

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